AVERAGE SMALL-SIGNAL ANALYSIS OF THE BOOST POWER FACTOR CORRECTION CIRCUIT

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ABSTRACT

A three-terminal, small-signal model for the boost power factor correction circuit is developed. The model is applicable for frequencies below the line frequency, and is useful for designing the low-frequency compensation network for feedback of the output voltage. The model is derived for a control with a reference derived either from the line or from a fixed sinusoidal reference. The implications of the new model are discussed for resistive and constant power loads, and design procedures for closing the voltage feedback loop are given.

I. Introduction

Many users of ac-dc power supplies are becoming increasingly conscious of the need to improve the power factor of the input current to the converter. One of the most common circuits used to achieve unity power factor is the boost converter. The operation of this converter has been analyzed in detail by many previous researchers, but none of them provides an averaged small-signal model suitable for the design and analysis of the output voltage feedback loop.

Fig. 1 shows a boost converter used with two different control schemes to achieve unity power factor. In the upper circuit, the switch is turned on until the inductor current equals a scaled multiple of the input voltage. A hysteresis comparator controls the off time. Fixed or variable hysteresis control can be used, but this does not affect the small-signal analysis. The lower circuit of Fig. 1 shows the same power stage, but the inductor current is compared to a fixed sinewave reference. It will be seen that this circuit has some small-signal advantages which may justify the more complex control needed to generate the fixed reference.

There are two major concerns of the small-signal performance of the circuit. Firstly, the control circuit forcing the line current to track the input voltage must be stable. This circuit can be analyzed in a manner very similar to state-space averaging, with the control voltage, v_c, and input voltage assumed constant during each switching cycle. The closed-loop eigenvalues of the circuit will vary as the input voltage increases from zero to its peak value. The second control consideration is the analysis of the

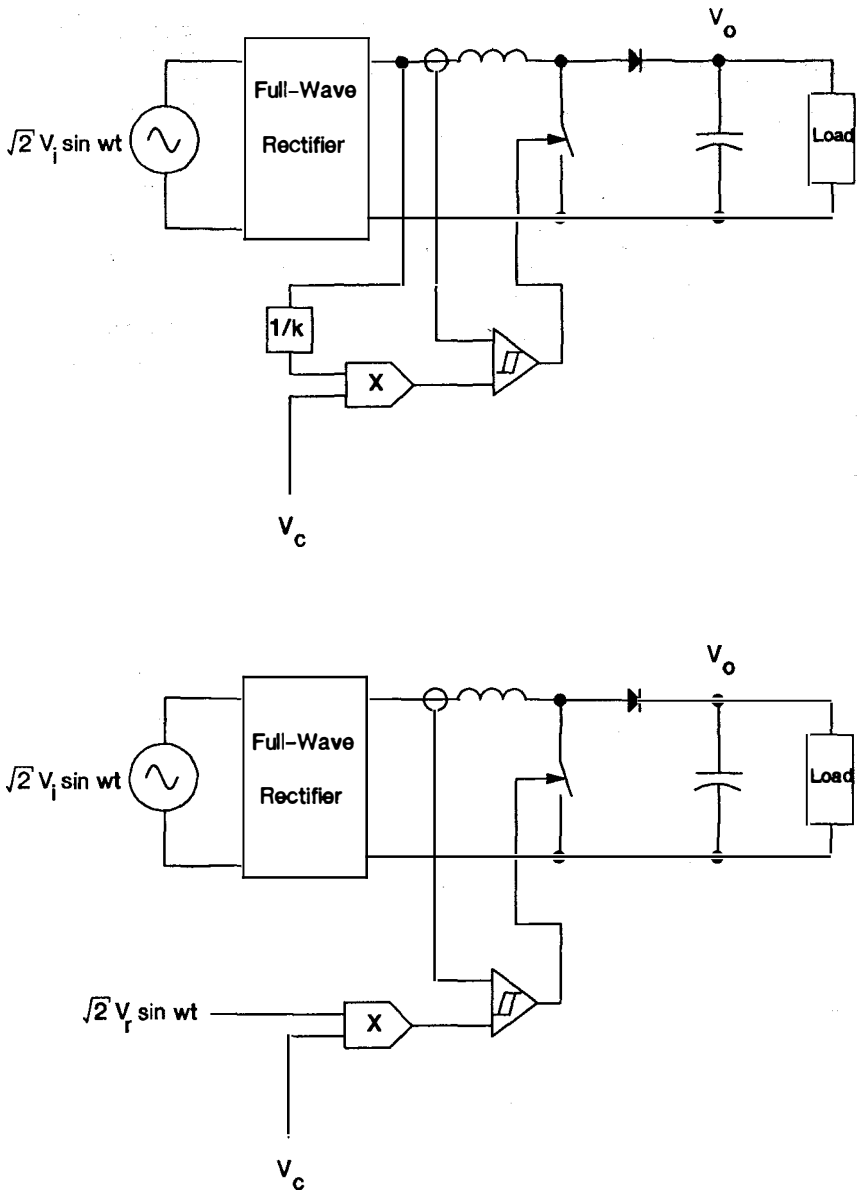

Figure 1. Boost Converter with Unity Power-Factor Control: The upper control circuit uses a line-voltage reference to control the inductor current. This provides a more sensitive control than the lower circuit, which uses an external reference synchronized to the input line frequency.

circuit on a cycle-to-cycle basis. In this case, the input current is assumed to track the input voltage correctly, and the circuit is analyzed on an average basis over a full cycle of operation. This analysis is essential for the proper design of the feedback circuit, which regulates the output voltage of the power factor circuit.

Many papers have discussed various implementations of active power factor correction circuits and dc-ac interfaces. Schlecht [1] introduced the concept of quasi-static analysis for these time-varying systems, and showed the locations of poles and zeros of the system as they changed over the sinusoidal cycle. Kocher and Steigerwald [2] analyzed a flyback version of the power factor cor-

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rection circuit, using a similar modeling technique, but the dynamics from control-input-to-output were not considered. Henze and Mohan [3] presented a control-output model consisting of a controlled current source feeding the load capacitor and resistor. This model is shown to be incomplete later in this paper. For resistive loads, this difference is small, but it can be significant with constant power loads. Mohan, Undeland and Ferraro [4] considered the current-programming loop of the boost converter, showing it to be stable for all conditions. Keller and Baker [5] correctly considered both the high-frequency current feedback loop and the low frequency output-voltage feedback, providing experimental measurements and SPICE simulations, which agreed well. Other papers [6,7] derive interesting topologies for isolating the power factor circuit or reducing semiconductor stresses.

The quasi-static analysis [4] of the boost converter with hysteretic current programming has been done, and is not considered in detail in this paper. No instabilities can arise in the current loop, and the only problem in designing the switching control circuit is in selecting an hysteresis scheme and finding a reliable method for sensing the line current. The design of the output-voltage compensator, however, has not been addressed, largely due to the lack of a small-signal model for the power converter on a cycle-to-cycle basis. This small-signal model is developed in this paper. Interesting differences to the model derived in [3] are shown, and the impact on design for resistive and constant-power loads is discussed. Design rules for the control components are given with consideration of widely-varying line and loads which can be encountered. The small-signal model and design guidelines are verified with computer simulation.

II. Small-Signal Analysis

The small-signal analysis is performed on an average basis over a complete half-cycle of the input sinewave voltage, assuming that the input current is properly controlled to track the scaled input voltage. This analysis uses similar techniques to those of Vorperian [7], who derived the equivalent PWM switch model for dc-to-dc converters. The waveforms of the converter are shown in Fig. 2. The input voltage is a sinewave, and the current-programming loop forces the input current to also be a sinewave. The output voltage is assumed to be constant over a switching cycle, and the output current is chopped at high frequency with a sinusoidal envelope equal to that of the input current. Referring to the waveforms of Fig. 2, the power balance equation for one cycle of operation is

$$v_i i_i = v_o i_o \tag{1}$$

The input quantities v_i and i_i are rms values, v_o is the dc output voltage, and i_o is the average output current over a cycle. For line-referenced control, shown in Fig. 1, the control law governing the input current is

$$i_i = \frac{v_i}{k} v_c \tag{2}$$

Substituting this control law into Eq. 1 gives

$$\frac{v_i^2}{k} v_c = v_o i_o \tag{3}$$

The steady-state conversion ratio, M, of the system can then be found:

$$M = \frac{V_o}{V_i} = \sqrt{\frac{V_c r_o}{k}} \tag{4}$$

where

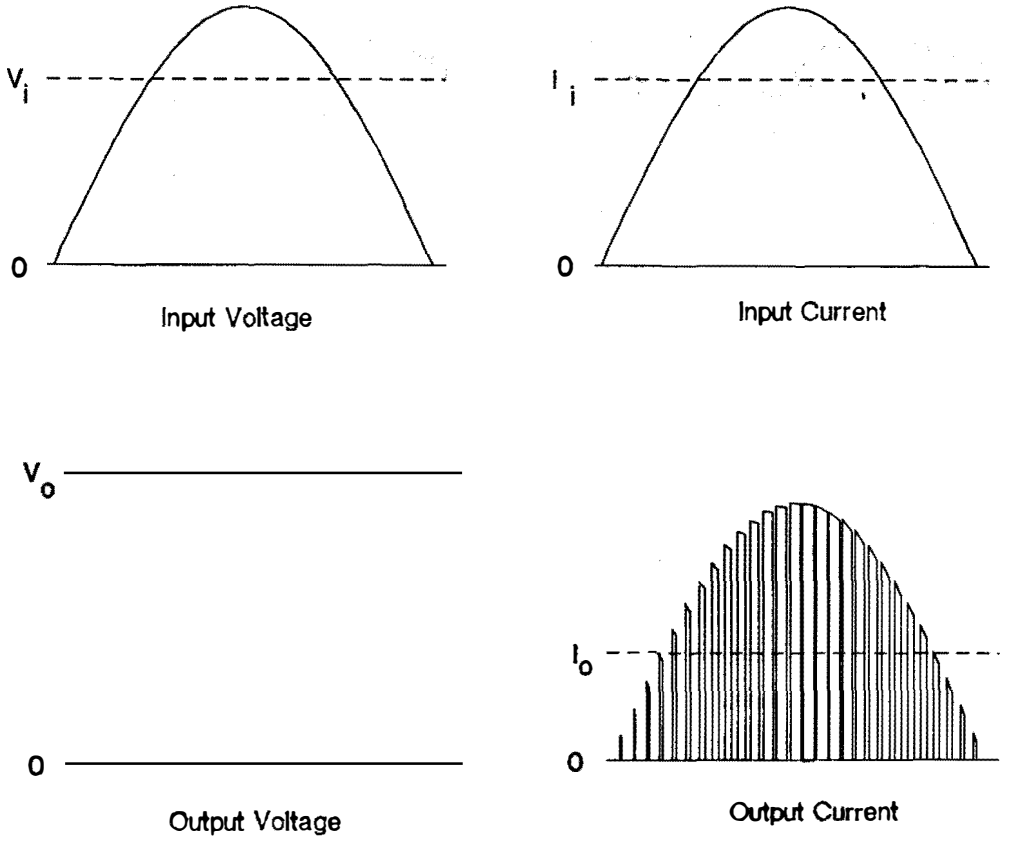

Figure 2. Waveforms of the Unity Power-Factor Boost Converter: The control circuit forces the input current to follow the input voltage sinewave. The average input and output terminal quantities of the power factor circuit are defined on the waveforms.

$$r_o = \frac{V_o}{I_o} \tag{5}$$

Perturbing Eq. 3 and eliminating small-signal cross-products and dc terms yields the equation

$$\hat{i}_o = \frac{2V_i V_c}{kV_o}\hat{v}_i + \frac{V_i^2}{kV_o}\hat{v}_c - \frac{I_o}{V_o}\hat{v}_o \tag{6}$$

which simplifies to

$$\hat{i}_o = \frac{2M}{r_o}\hat{v}_i + \frac{V_i}{kM}\hat{v}_c - \frac{1}{r_o}\hat{v}_o \tag{7}$$

The control Eq. 2 can be similarly perturbed to give

$$\hat{i}_i = \frac{V_i}{k}\hat{v}_c + \frac{M^2}{r_o}\hat{v}_i \tag{8}$$

III. Equivalent Small-Signal Circuit

The small-signal Eqs. (7) and (8) can be represented with the simple circuit model shown in Fig. 3. The component values of this circuit are all given in the left column of Table 1. Similar analysis can be performed for the fixed-reference control scheme of Fig. 1, and the component values corresponding to

this circuit are in the right-hand column of Table 1. The small-signal equivalent circuit remains the same for both control schemes. Notice that this circuit is not a simple controlled current source feeding the load, due to the presence of the small-signal resistor r_o .

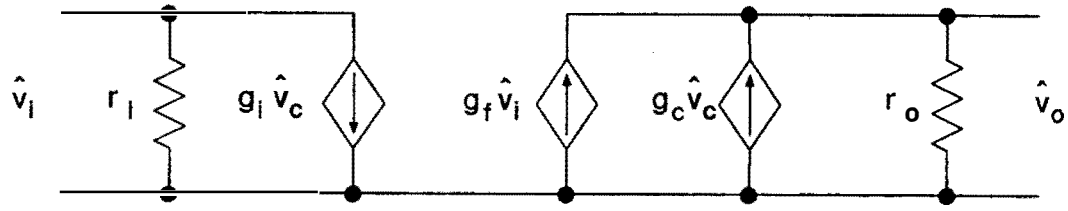

Figure 3. Small-Signal Circuit Model of the Boost Power Factor Circuit: This circuit models the small-signal Eqs. (7) and (8). Notice the presence of the small-signal output resistor, r_o, which significantly affects the characteristics of the circuit when connected to a resistive or a regulator load.

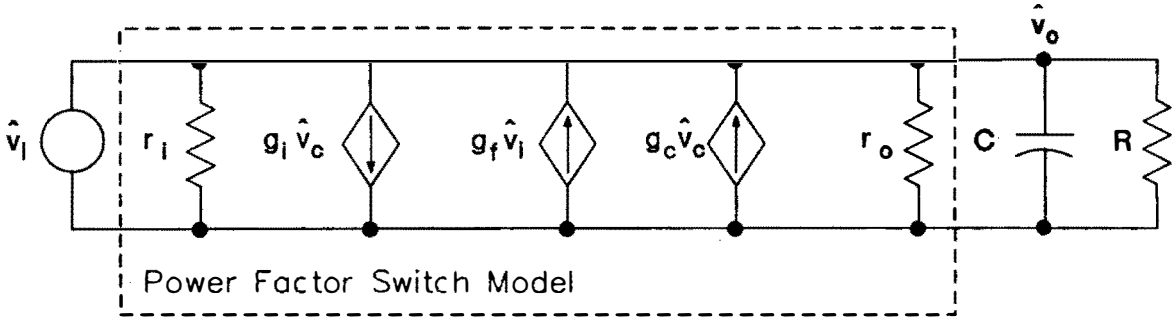

Figure 4. Small-Signal Circuit Model with Output Filter Load: The small-signal model of Fig. 4 is connected to the external load and input source.

From the small-signal circuit of Fig. 4 with the output filter capacitor and load connected, the input-output transfer function can be derived by inspection to give

$$\frac{\hat{v}_o}{\hat{v}_i} = g_f \frac{r_o // Z_L}{1 + sCr_o // Z_L} \tag{9}$$

Similarly, the control-output transfer function can be derived by inspection to give

$$\frac{\hat{v}_o}{\hat{v}_c} = g_c \frac{r_o // Z_L}{1 + sCr_o // Z_L} \tag{10}$$

For a resistive load R_L, the small-signal resistance r_o is equal to the load resistance, and the control-output transfer function simplifies to

Table 1. Small-Signal Component Values for the Boost Power Factor Correction Circuit.

	LINE REFERENCE	FIXED REFERENCE
M	$\sqrt{\frac{V_c r_o}{k}}$	$\sqrt{\frac{V_r V_c r_o}{V_i}}$
r_i	$\frac{r_o}{M^2}$	∞
g_i	$\frac{V_i}{k}$	V_r
r_o	$\frac{V_o}{I_o}$	$\frac{V_o}{I_o}$
g_f	$\frac{2M}{r_o}$	$\frac{M}{r_o}$
g_c	$\frac{V_i}{kM}$	$\frac{V_r}{M}$

$$\frac{\hat{v}_o}{\hat{v}_c} = g_c \frac{R_L}{2 + sCR_L} \tag{11}$$

Notice that the time constant of this expression is half that which would be expected without the small-signal resistance r_o.

A constant power load, such as a switching regulator, has a small-signal input impedance at low frequencies given by [8]

$$R_i = -\frac{V_o}{I_o} \tag{12}$$

where V_o and I_o are the input voltage and current, respectively, of the regulator, provided by the output of the power-factor correction circuit. The control-output transfer function of the power-factor correction circuit when connected to a regulator load is

$$\begin{aligned} \frac{\hat{v}_o}{\hat{v}_c} &= g_c \frac{r_o // -R_i}{1 + sCr_o // -R_i} \\ &= g_c \frac{1}{sC} \end{aligned} \tag{13}$$

In this case, the small-signal resistance is of opposite sign to the input resistance of the regulator, and the parallel combination is an open circuit. This is significantly different from the small-signal model of [3], with the controlled current source feeding the load. Fig. 5 shows the control-output plots for the model with and without r_o .

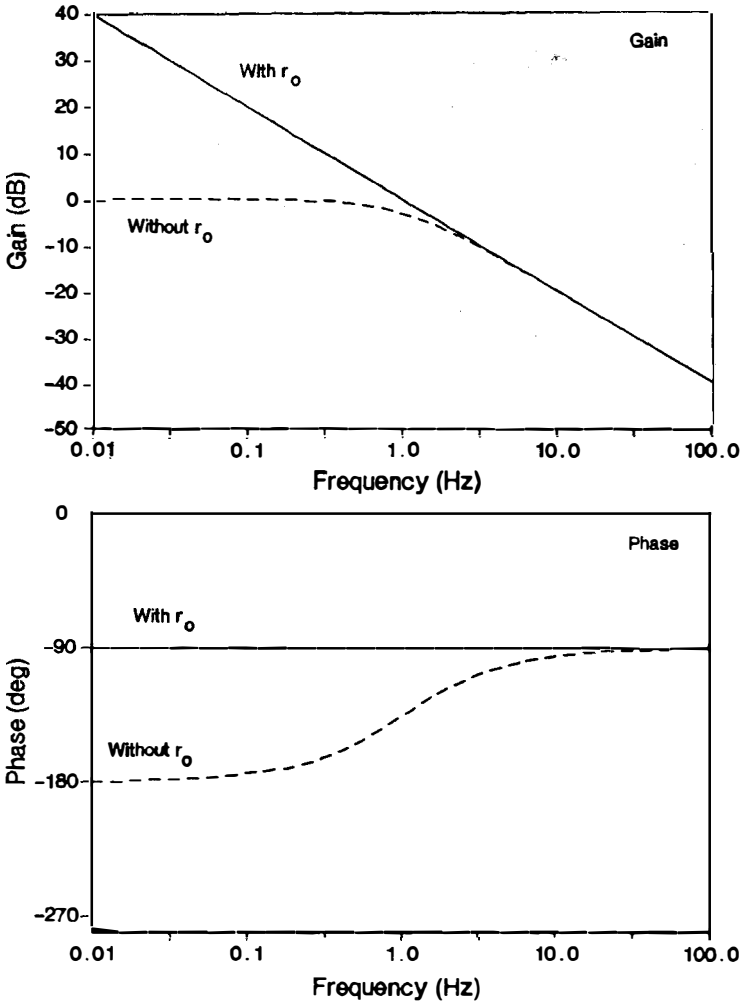

Figure 5. Control-Output Transfer Function with Regulator Load: The significance of the small-signal resistance r_o when the circuit supplies a constant power load is demonstrated by the plot with and without this resistor in the model.

The system model without r_o is open-loop unstable, with a right-half plane pole at $s = 1/CR_L$. The model with r_o does not have the right-half plane pole, and has the characteristics of an integrator. The model without r_o has severe implications for the control compensation which must be used. It is desirable to use an integrator and lead network to produce low dc error. However, such a compensation would produce a conditionally stable system where the phase exceeds -180° at low frequencies, and is less than 180° at crossover, as shown in Fig. 6. Such a system is undesirable due to reductions in gain which can be encountered during transient or start-up conditions.

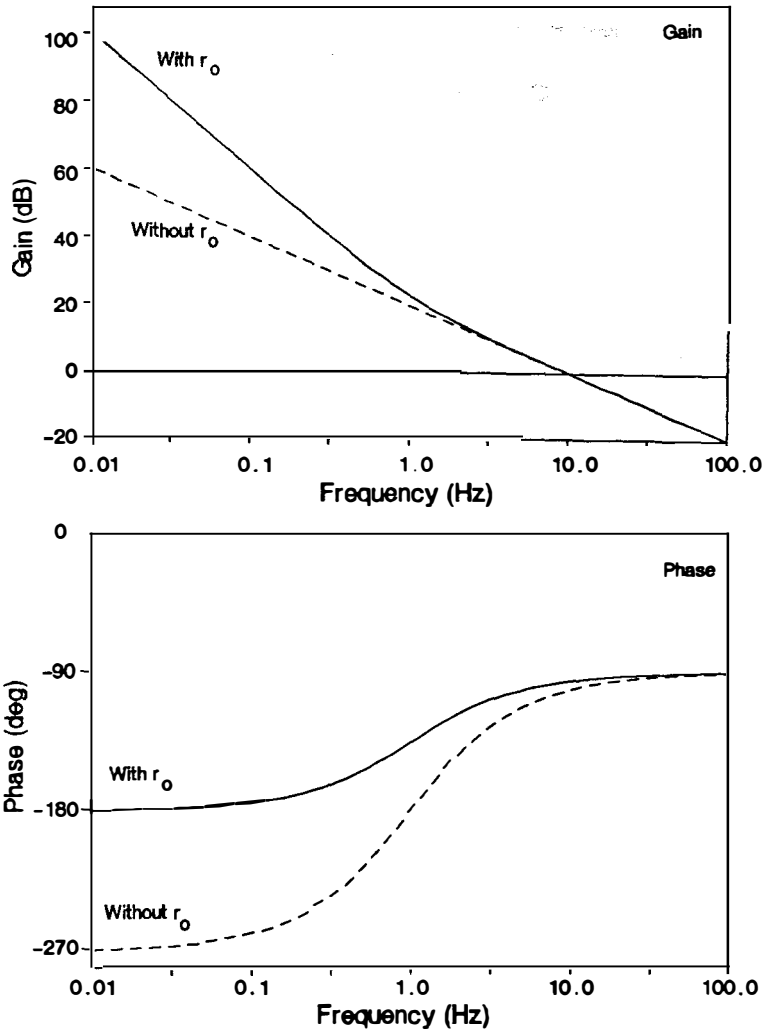

Figure 6. Compensated Loop Gain with Regulator Load: The significance of the small-signal resistance r_o on the loop gain with a constant-power load is demonstrated.

IV. Verification of Small-Signal Model

The small-signal model can be verified by simulating the exact switching circuit, and comparing the output-voltage transient with that predicted by the small-signal equivalent circuit. A 50-W circuit was used as an example, with the parameter values defined in Table 2, assuming a resistive load, and a filter capacitor of 673 μF. Line-referenced control was used for the simulation. From Eq. 9, the line-to-output transfer function is

$$\frac{\hat{v}_o}{\hat{v}_i} = g_f \frac{R_L}{2 + sCR_L} = \frac{2M}{2 + sCR_L} = \frac{2}{1 + 0.0673s} \quad (14)$$

The time-domain response for the output voltage is then given by

Table 2. Numerical Values for the Small-Signal Components of Design Example

	LINE REFERENCE	FIXED REFERENCE
V_i	50	50
V_o	100	100
I_o	0.5	0.5
V_c	1	1
k	50	-
V_r	-	1
M	2	2
r_i	50	∞
g_i	1	1
r_o	200	200
g_f	0.02	0.01
g_c	0.5	0.5

$$v_o(t) = V_o + 2\Delta V_i\left[1 - e^{-14.86t}\right] = 100 + 10\left[1 - e^{-14.86t}\right] \quad (15)$$

for a 5-V step input change.

Fig. 7 show the exact digital simulation of this example superimposed on the step response predicted by Eq. (15). It can be seen that the small-signal model predicts the correct result. Similarly, for a step control change of 0.1 V, the output voltage transient from the small-signal model is

$$v_o(t) = 100 + 5\left[1 - e^{-14.86t}\right] \quad (16)$$

The results of the exact simulation and the prediction of the small-signal model are shown in Fig. 8 for a step change in the control voltage. The excellent agreement of the results confirms the validity of the small-signal modelling.

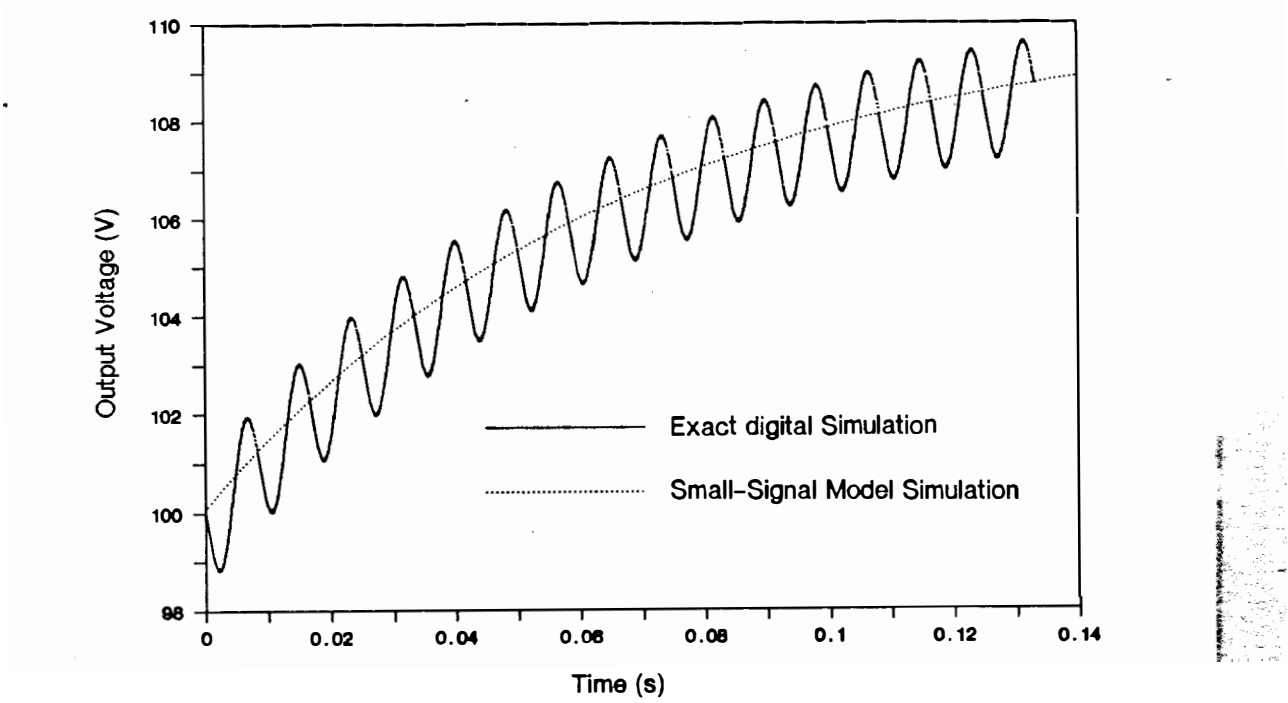

Figure 7. Simulated Circuit Response for a Step-Line Change: The exact simulation of the circuit closely follows the response predicted by the small-signal model, verifying the time constant and amplitude of the first-order system response.

V. Feedback Loop Compensation

Feedback compensation is required to regulate the output voltage over the full input voltage and output load range. An integral-and-lead network provides the optimum compensation for both resistive and constant power loads. Two parameters must be selected for the compensation network: the location of the zero, and the high-frequency gain. These parameters are defined on the compensation gain asymptotes shown in Fig. 9. For a resistive load, the zero should be placed at the same frequency as the pole in the transfer function from control to output, given by

$$\omega_z = \frac{2}{CR_L} \tag{17}$$

This location of the compensation zero ensures a 90° phase margin at all frequencies for a resistive load.

The transfer function from control-output with a constant power load (Fig. 6) is simply an integrator. The zero for this case must be placed at or below the minimum crossover frequency of the loop gain to provide a phase margin of 45° or greater. The control-output transfer function is

$$\frac{\hat{v}_o}{\hat{v}_c} = g_c \frac{1}{sC} = \frac{V_i}{kM} \frac{1}{sC} \tag{18}$$

for line-referenced control, and

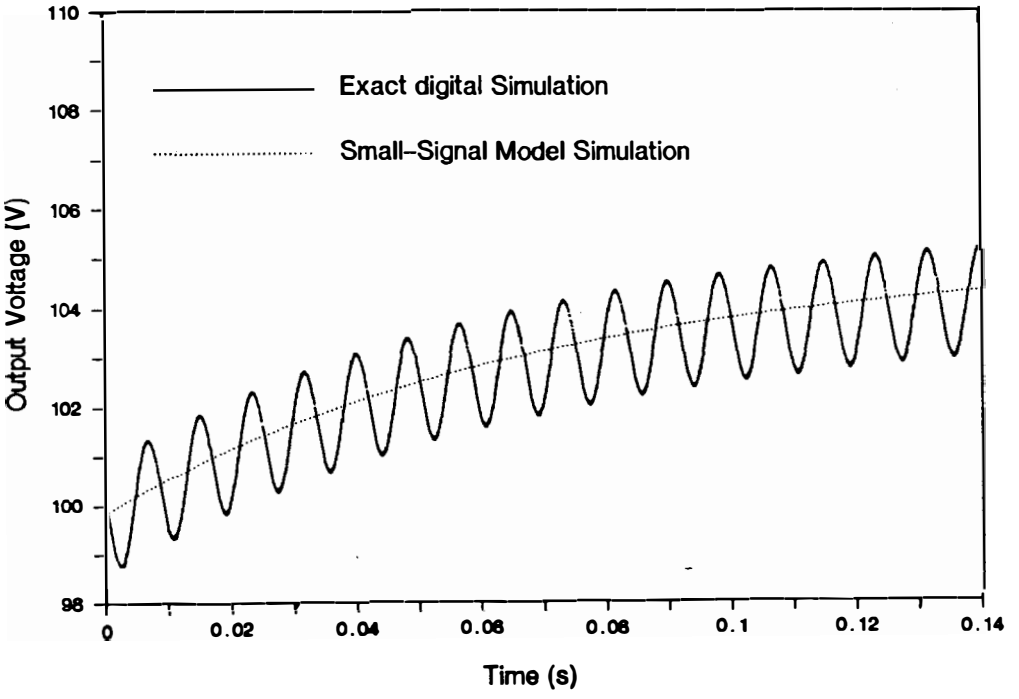

Figure 8. Simulated Circuit Response for a Step-Control Change: The exact simulation of the circuit closely follows the response predicted by the small-signal model, verifying the time constant and amplitude of the first-order system response.

$$\frac{\hat{v}_o}{\hat{v}_c} = g_c \frac{1}{sC} = \frac{V_r}{M}\frac{1}{sC} \tag{19}$$

for a constant-reference control. Both of these transfer functions change with line conditions, but not with load variations, and have a maximum value at high line. A suitable crossover frequency at high line is 1/4 the frequency of the rectified line, or 1/2 the frequency of the input line. The high-frequency asymptote can then be selected for the compensation:

$$\begin{aligned} k_c &= \omega_l C \frac{1}{2g_c} \\ &= \omega_l C \frac{kM_{\min}}{2V_i^{\max}} \end{aligned} \tag{20}$$

for line-referenced control and

$$k_c = \omega_l C \frac{M_{\min}}{2V_r} \tag{21}$$

for fixed reference control. In both cases, the maximum crossover frequency of loop gain will be given by

$$\omega_c^{max} = \frac{\omega_l}{2} \tag{22}$$

The minimum crossover frequency, occurring at low line, is given by

$$\omega_c^{min} = \left[\frac{V_i^{\min}}{V_i^{max}}\right]^2 \frac{\omega_l}{2} \tag{23}$$

for line-referenced control and

$$\omega_c^{min} = \frac{V_i^{min}}{V_i^{max}} \frac{\omega_l}{2} \tag{24}$$

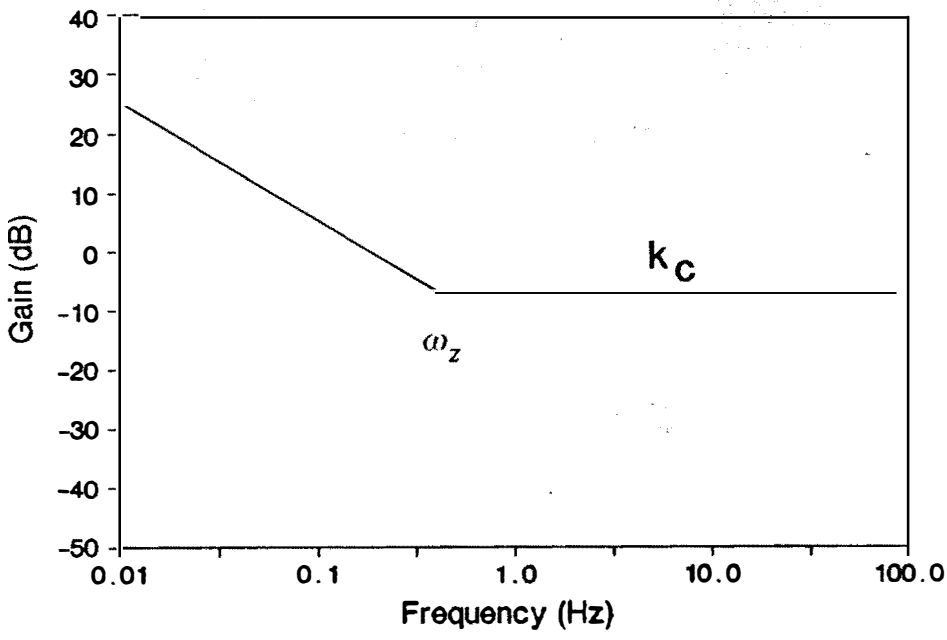

Figure 9. Compensation Gain Asymptotes: An integral and lead network is used to provide zero dc error and good phase margin at the crossover frequency. The zero of the compensation network is placed before the crossover frequency.

for fixed-reference control. The flat gain of the compensation network at higher frequencies will transmit considerable ripple back to the control voltage, v_c, which can distort the input waveforms. However, this ripple can easily be removed with the addition of a notch filter at twice the line frequency. The design of such a compensation scheme is not considered in this paper.

The zero of the compensation network should be placed at ω_c^{min} for a 45° phase margin, or, more conservatively, at $\frac{2}{\sqrt{3}}\omega_c^{min}$ for a 60° phase margin. The recommended zero locations and gains of compensators for the different control schemes with resistive and constant-power loads are summarized in Table 3.

Table 3. Recommended Compensation Circuit Parameter Values

	LINE REFERENCE		FIXED REFERENCE	
	Resistive	Regulator	Resistive	Regulator
ω_z	$\frac{2}{CR_L}$	$\frac{\omega_l}{\sqrt{3}}\left[\frac{V_i^{min}}{V_i^{max}}\right]^2$	$\frac{2}{CR_L}$	$\frac{\omega_l}{\sqrt{3}}\frac{V_i^{min}}{V_i^{max}}$
k_c	$\omega_l C\frac{kM_{\min}}{2V_i^{max}}$		$\omega_l C\frac{M_{\min}}{2V_r}$	

VI. Conclusions

An average small-signal circuit model has been developed to predict the response of the boost power-factor correction circuit. Simulated results for step-line and step-control transients have confirmed the results of the small-signal modeling. The circuit model contains a small-signal resistance, r_o, which significantly affects the performance of the circuit, simplifying the compensation design when a regulator is preceded by the power factor correction circuit.

Control-loop compensation design procedures have been developed for two different power-factor control schemes, with either resistive or constant power loads. The design guidelines provide a simple, non-iterative procedure for the selection of control parameters, which can easily be automated by a computer program. The next phase of this work will use these results to close the loop on simulated and hardware converters, to verify the small-signal model and design procedures.

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