Multi-Loop Control for Quasi-Resonant Converters

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Abstract—**A new, multi-loop control scheme for quasi-resonant converters is described. Similar to current-mode control for PWM converters, this control offers excellent transient response and replaces the voltage-controlled oscillator with a simple comparator. A signal proportional to the output-inductor current is compared with an error voltage signal to modulate the switching frequency. The control can be applied to either zero-voltage-switched or zero-current-switched quasi-resonant converters. Computer simulation is used to demonstrate the effectiveness of the control method applied to a zero-current-switched buck quasi-resonant converter. Experimental results are presented for zero-current flyback and zero-voltage buck quasi-resonant converters, operating at up to 7 MHz.**

I. Introduction

QUASI-RESONANT converters (QRC's) eliminate much of the switching loss encountered in pulsewidth modulation (PWM) converters since the active device is switched with either zero current or zero voltage at its terminals. This allows for circuit operation at frequencies above one megahertz. Many different QRC topologies have been presented and their power circuit operation analyzed [1]–[5.] QRC's are controlled by varying the switching frequency. Closed-loop regulation is most commonly achieved by feedback of the output voltage through an error-amplifier circuit and a voltage-controlled oscillator (VCO). This is analogous to constant off-time duty-cycle modulation of a single-loop-controlled PWM converter.

Small-signal analysis of QRC's [4] shows that their low-frequency characteristics are similar to those of their PWM converter counterparts. It can be difficult to achieve satisfactory closed-loop response with single-loop control, especially for boost and buck-boost derived circuits with a right-half-plane zero in their control-to-output transfer functions. Current-mode control offers significant improvement in closed-loop response for PWM converters [6]. The purpose of this paper is to present a similar scheme for the control of QRC's. Referred to as current-sense frequency modulation (CSFM), this control compares a signal proportional to the output-filter inductor current with an error voltage signal to modulate the switching frequency.

The applications of CSFM are described in this paper for a zero-current-switched (ZCS) buck QRC, ZCS flyback QRC, and zero-voltage-switched (ZVS) buck QRC. Simulated and experimental circuit waveforms are given, and the closed-loop transient responses for step changes of input voltage and load current are compared to those with single-loop control for the ZCS buck converter. Small-signal loop gain measurements are presented.

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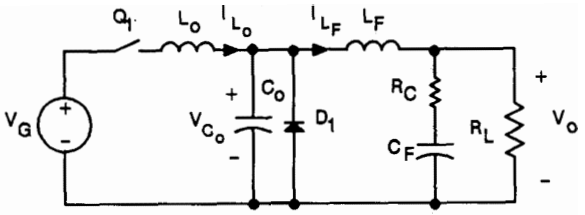

Fig. 1. Quasi-resonant buck converter power stage. L_o = 30 nH; C_o = 0.3 μF; L_F = 5.7 μH; C_F = 63 μF; R_C = 10 mΩ; R_L = 0.5 Ω; V_G = 12 V; V_o = 5 V; F_s = 400 kHz.

II. ZCS QRC Power Stage Operation

Before describing the new control scheme, the power stage operation of a ZCS quasi-resonant buck converter is reviewed. Fig. 1 shows the circuit diagram of this converter. The output stage of the circuit, formed by components L_F, C_F, R_C and R_L, is identical to that of the PWM buck converter. The simple switching cell of the buck converter, however, is replaced by a resonant switch formed by the components Q_1, L_0, C_0 and D_1. If switch Q_1 is current bidirectional, the circuit is operated in full-wave mode; otherwise, with switch Q_1 unidirectional, the circuit is operated in half-wave mode [1].

Operation of the circuit is best understood by considering each linear circuit formed during a cycle of operation. Fig. 2 shows the topologies formed by the different switch conditions, and gives the circuit conditions which define when each topology is terminated. Each mode es entered sequentially for continuous current in the output filer inductor. During topology I, both the power switch and diode are conducting, and the resonant inductor current increases linearly until it equals the filter inductor current. The diode then turns off, and the resonant cycle of the circuit is entered during topology II.

For half-wave operation, the power switch is turned off when the resonant inductor current reaches zero, and the resonant capacitor discharges into the load filter in topology III. The final topology is entered when the resonant capacitor voltage falls to zero, and the diode again conducts. Control of the circuit is achieved by regulating the time off time of the power switch Q_1.

The simulated steady-state circuit waveforms are shown in Fig. 3. The component values of the power circuit for all simulation results are given in Fig. 1. The output-filter inductor-current waveform is similar to that of a PWM converter. During topology IV, when the control must be implemented, the inductor current decreases linearly.

III. Single-Loop-Controlld QRC

Closed-loop regulation of the output voltage of a QRC can be achieved by feedback of the output voltage. The small-signal analysis [4] shows that the quasi-resonant power stages have

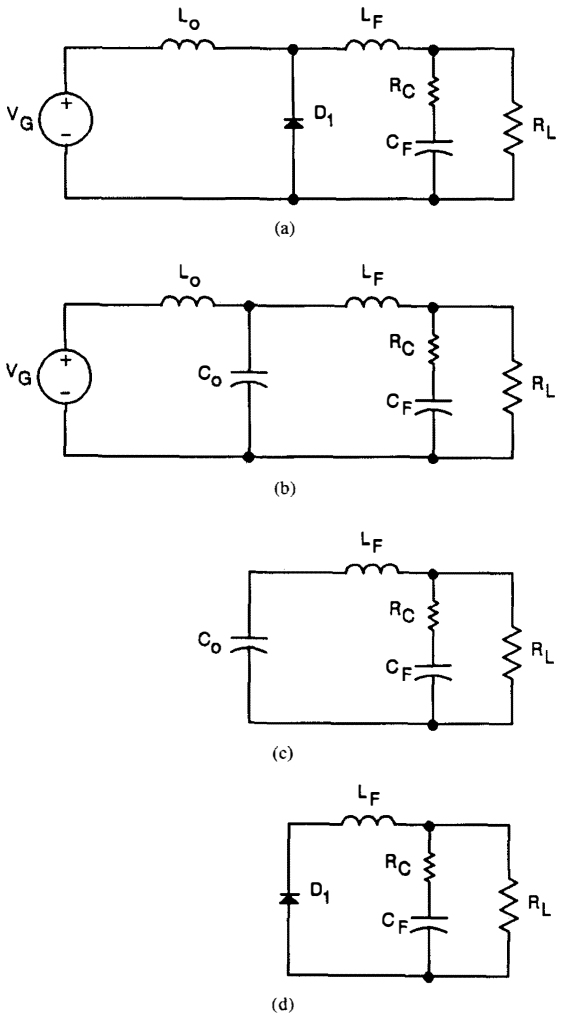

Fig. 2. Topological modes of half-wave quasi-resonant buck converter during continuous-current operation, and conditions for exciting each mode. (a) Topology I. Linear charging topology, ended when $I_{L_o} = I_{L_F}$. (b) Topology II. Resonant topology, ended when $I_{L_o} = 0$. (c) Topology III. Capacitor discharge topology, ended when $V_{C_o} = 0$. (d) Topology IV. Freewheeling topology, ended by control signal.

low-frequency characteristics similar to those of their PWM counterparts. The resonant elements can significantly affect the small-signal characteristics in the high-frequency region, depending on the placement of the components, but these effects are not considered in this paper. A compensation network can therefore be designed in a similar manner to that of a PWM converter to meet the closed-loop performance specifications. A commonly used, single-loop control scheme for the buck QRC power stage described earlier is shown in Fig. 4. A two-pole, two-zero compensation network is used for this circuit to provide high low-frequency gain and good phase margin at the crossover frequency.

The output of the error amplifier controls the VCO which determines the off-time of Q_1. Control logic, DSP (digital signal processor), consists of switch-drive circuitry and logic which converts the output signal of the VCO into a constant on-time pulse. The signal at the output of the error amplifier is shown in Fig. 6(a). This single-loop control has several disadvantages. The crossover frequency of single-loop-controlled QRC's is limited, as for PWM converters, and the undamped buck QRC and the boost and buck-boost QRC's can be very difficult to compensate. Crossover frequency and good closed-loop performance must be traded off against stability. Single-loop control is also sensitive to power-stage parameter variations, and the converter can be difficult to stabilize with good performance for all operating conditions and component variations.

IV. Multi-Loop-Controlled QRC

Multi-loop control (or current-mode control) is effective for controlling PWM converters, providing good stability margin, and high crossover frequency. For QRC's, CSFM offers the same advantages. In addition, the VCO used for single-loop control of QRCs is replaced with a comparator. Fig. 5(a) shows the basic concept for implementation of CSFM for the buck QRC. The continuous filter inductor current is sensed directly. The control waveforms for this implementation of CSFM are shown in Fig. 6(b). When the downslope of this current intersects the control error voltage, the power switch is turned on. Using this multi-loop control, the circuit can be stabilized with a single-zero, two-pole compensation network.

Like current-mode control for PWM converters [6], several possible ways of implementing CSFM exist. The most direct method uses resistive sensing with an operational amplifier, but this is inefficient, and impractical for high-current outputs. A second method uses a current transformer in series with diode D_1, as shown in Fig. 5(b). A current transformer can be used here since the diode current is equal to the filter inductor current during topology IV, and its discontinuous waveform allows reset of the current transformer core. The control waveforms for this circuit are shown in Fig. 6(c). This control implementation offers current sharing and current limiting, but the high-amplitude step current waveforms generate considerable noise. This problem is frequently encountered when using current-injection control for PWM converters [6], and is worse at the higher switching frequencies of QRC's. Also, when sensing the off-time diode current, the positive edge of the sensed waveform must be ignored by the control circuit, and the switch should be turned on again only when the negative slope intersects the control threshold.

If current limiting is implemented separately, and current sharing is not required, the most simple and effective implementation of CSFM can be achieved as shown in Fig. 5(c). Here, the inductor voltage is sensed with an auxiliary winding on L_F and integrated through R_3 and C_1 to reconstruct the inverted ac portion of the inductor current. This is summed through the operational amplifier with the error voltage and compared to a fixed reference. The control waveforms for this circuit are shown in Fig. 6(d). This implementation of CSFM is analogous to the standard control module (SCM) for constant on-time PWM converters [6]. The circuit provides very clean control signals due to the integration of all control waveforms, and is the most useful for high-frequency QRC's. All three implementations of CSFM offer identical small-signal characteristics and transient response of the circuit.

V. Simulated Closed-Loop Transient Response

The single-loop circuit of Fig. 4 and the multi-loop circuit of Fig. 5(a) were simulated to demonstrate the effectiveness of the

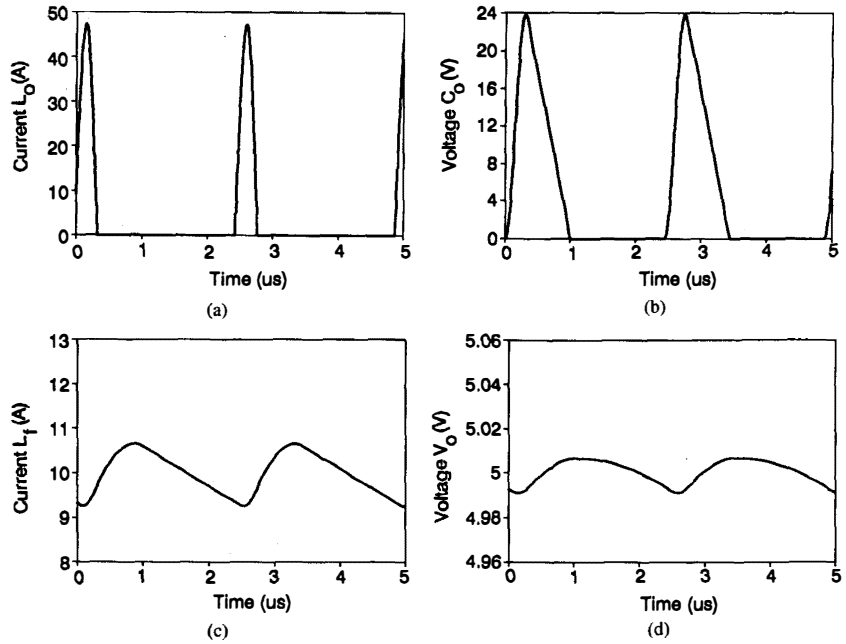

Fig. 3. Steady-state power stage waveforms for half-wave mode operation (a) Resonant inductor current. (b) Resonant capacitor voltage. (c) Filter-inductor current. (d) Output voltage.

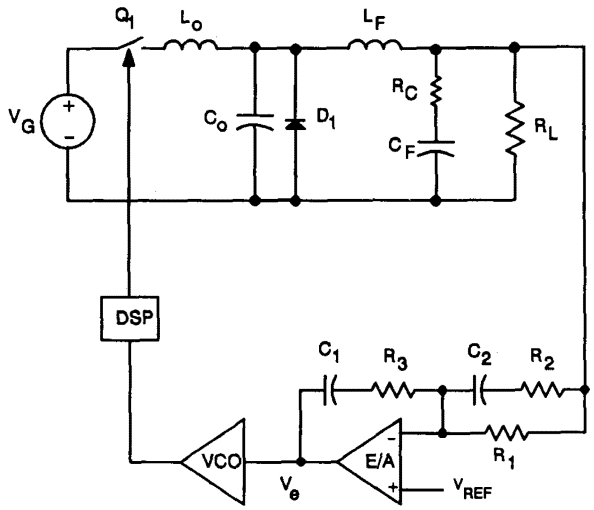

Fig. 4. Single-loop-controlled QRC with voltage-controlled oscillator. C_1 = 800 pF; C_2 = 6300 pF; R_1 = 3.1 kΩ; R_2 = 1.0 kΩ; R_3 = 10 kΩ; VCO gain; = 0.32 MHz/V.

new control scheme. Long-term simulations [7] were performed to show the transient response to a 25% step input voltage and a 10% step load. Every effort was made to design the control loop to give the best possible transient response for both single-multi-loop control schemes.

The response of the CSFM-controlled buck converter to a 25% step input voltage is shown in Fig. 7(a), and the response to a step-load current in Fig. 8(a). The step change occurred after 50 μs. The 5-V output had an overshoot of 23 mV for the step input, and 28 mV for the step load, both with a settling time of less than 60 μs.

The step-line and step-load responses of the single-loop-controlled converter are shown in Figs. 7(b) and 8(b). The peak overshoot for a step line was 46 mV, and the step-load transient shows the oscillatory response of the control system, indicating an insufficient phase margin.

The control compensation was simple to design with CSFM and stable over a wide range of input voltage and parameter

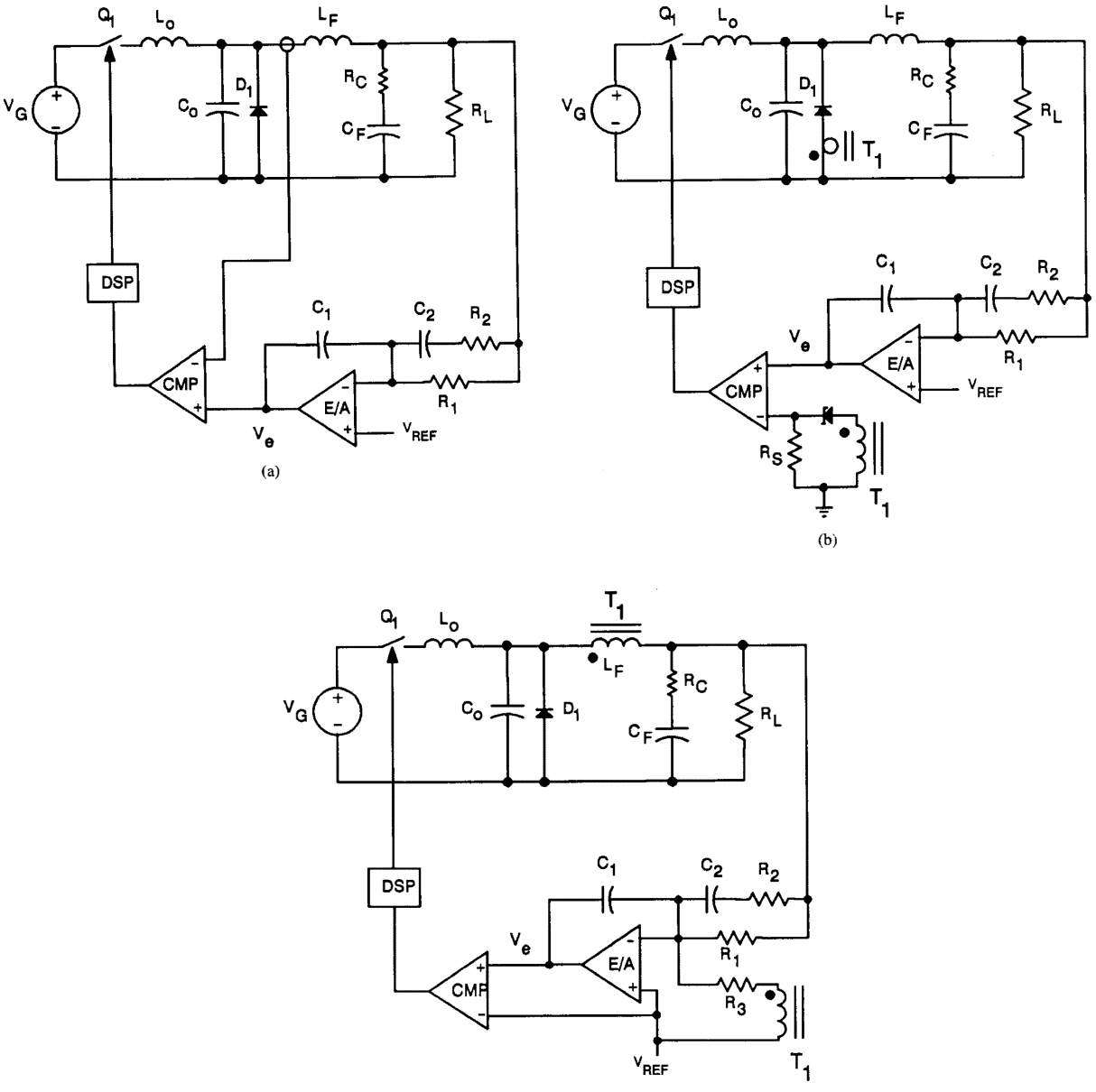

Fig. 5. CSFM-controlled ZCS buck QRC. C_1 = 200 pF; C_2 = 6300 pF; R_1 = 3.1 kΩ; R_2 = 100 Ω; V_r = 5.0; Current sense gain = 1. (a) Direct inductor current sensing. (b) Diode current sensing. (c) AC current sensing.

variations. The very stable response to step transients shows more than adequate stability, indicating that the gain could have been increased at the expense of some phase margin. The compensation for single-loop control was more complex to design and much more sensitive to variations of line, load and power-stages components, actually becoming unstable under some operating conditions. There is no margin for improved performance in this design.

VI. Multi-Loop Control for 10 MHz Converters

CSFM has been successfully implemented for applications with switching frequencies up to 1 MHz, using an operational amplifier to integrate the power stage inductor voltage. Beyond this frequency, it is difficult to obtain a clean waveform at the output of the operational amplifier. The open-loop voltage gain of a LF356 amplifier (National Semiconductor) is shown in

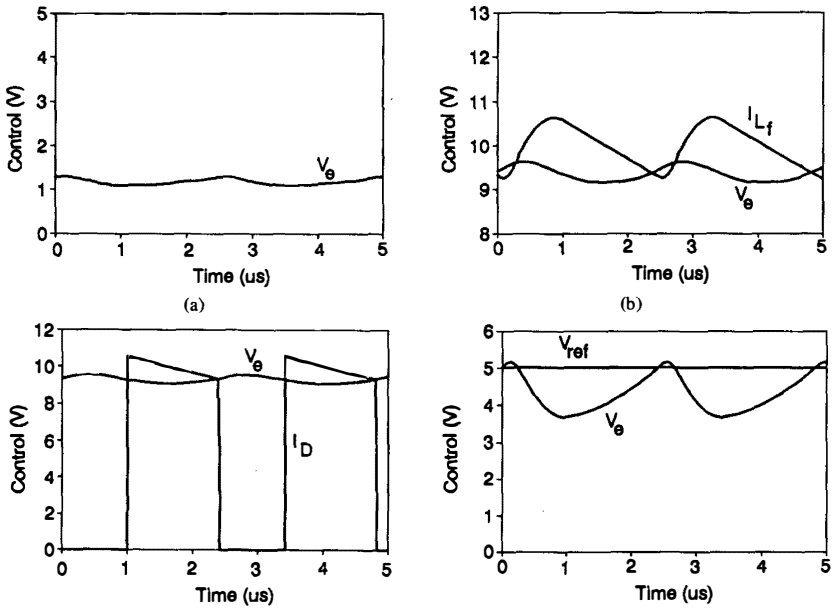

Fig. 6. Simulated steady-state control waveforms. (a) Single-loop control error voltage. (b) CSFM with direct current sensing. (c) CSFM with diode current sensing. (d) CSFM with ac current sensing.

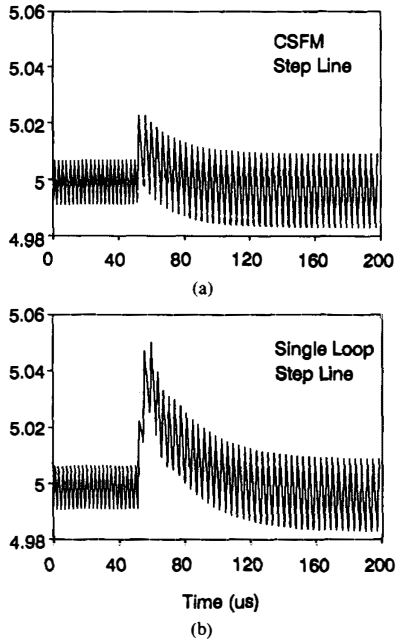

Fig. 7. Simulated step-line (25%) response of ZCS buck QRC. (a) CSFM control. (b) Single-loop control.

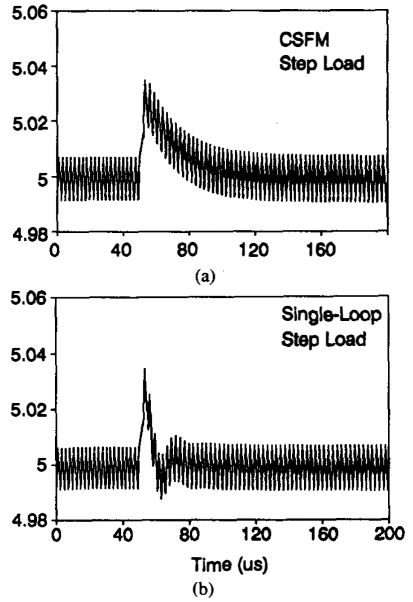

Fig. 8. Simulated step-load (1A) response of ZCS buck QRC. (a) CSFM control. (b) Single-loop control.

Fig. 9. Its limited bandwidth, limited slew rate, and finite response time prevent it from effectively integrating the square-wave inductor voltage at frequencies above 1 MHz. Higher-performance amplifiers could be used, but these are usually very sensitive to high-frequency noise. There are also limitations on the logic circuit used at 1 MHz. Since the CSFM control regulates the switching frequency on a pulse-by-pulse basis, the response time of the comparator and control logic must be short compared to the on-time of the circuit. An alternative to active integration of the inductor voltage must be found to apply this control at frequencies up to 10 MHz.

The small-signal block diagram of the multi-loop-controlled

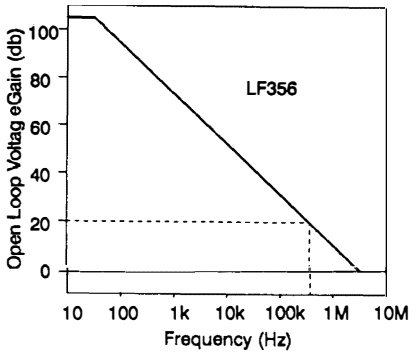

Fig. 9. Typical bode plot of LF356 operational amplifier.

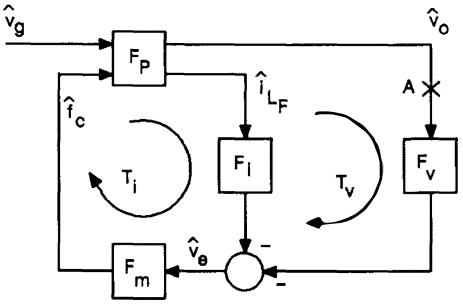

Fig. 10. Small-signal block diagram of CSFM-controlled QRC.

power stage is shown in Fig. 10. The gain block F_p represents the power-stage characteristics. The block F_v is determined by the voltage compensation, and F_m, the modulator gain, is determined by the slope of the control ramp. The current-sense gain is represented by F_i. For the circuit of Fig. 5(c), this gain is given by

$$F_i = snL \cdot \frac{1}{sR_3C_1} = \frac{nL}{R_3C_1} \tag{1}$$

where n is the ratio of inductor sense turns to inductor power turns. The small-signal gain of the current sense feedback is constant, with no frequency dependence. In developing a circuit for higher frequencies, this constant gain must be maintained.

The passive RC network shown in Fig. 11 can be used to integrate the high-frequency component of the inductor voltage. This network produces a clean ramp at frequencies beyond 10 MHz, and provides a very simple solution to the problem. A second sensing winding must be used on the output-filter inductor to provide an isolated signal to the RC network. The gain of the sensing network of Fig. 11 is

$$F_i'' = \frac{sK''}{s + a''} \tag{2}$$

where

$$K'' = \frac{n''L}{C_3R_3} \tag{3}$$

and

$$a'' = \frac{1}{C_3R_3}. \tag{4}$$

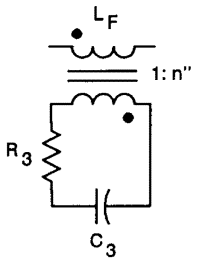

Fig. 11. Passive RC network for high-frequency integration of filter-inductor voltage.

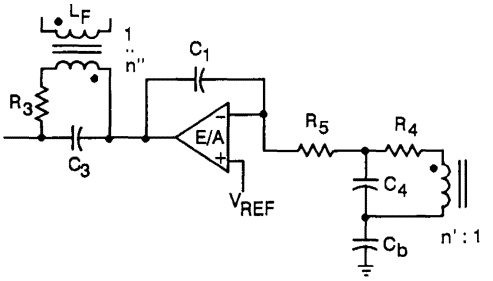

Fig. 12. Combined current-sensing network for integration of filter-inductor voltage.

The passive network does not give constant gain due to the pole at the R_3C_3 corner frequency. It does, however, integrate at frequencies above this corner, and can be used to provide high-frequency feedback which cannot be provided by an amplifier circuit. To regain the constant gain required of the current feedback, an amplifier network can be used as before with the addition of an extra pole at the same frequency as the pole of the high-frequency feedback network. An operational amplifier network providing low-frequency feedback of the inductor current is shown in Fig. 12, with the high-frequency feedback network. The gain from the inductor current to the output of the amplifier is given by

$$F_i' = \frac{K'}{s + a'} \tag{5}$$

where

$$K' = \frac{n'L}{C_4C_1R_5R_4} \tag{6}$$

and

$$a' = \frac{1}{C_1(R_5//R_4)}. \tag{7}$$

The small-signal block diagram of a converter with this current-sensing scheme is shown in Fig. 13. Two current-feedback loops are used to give the same characteristics as the control system shown in Fig. 10. The gain $F_i = F_i' + F_i''$ can be made a constant for all frequencies if the components of the current sensing circuit of Fig. 12 are chosen correctly.

VII. Experimental Results

A. 1-MHz Flyback ZCS QRC

Two hardware circuits have been implemented to verify the performance of CSFM control. Fig. 14 shows the application

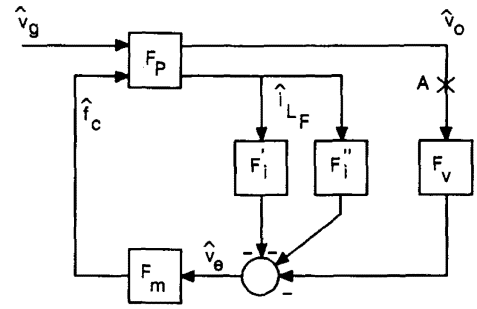

Fig. 13. Small-signal block diagram of CSFM-controlled QRC with two-loop current sensing.

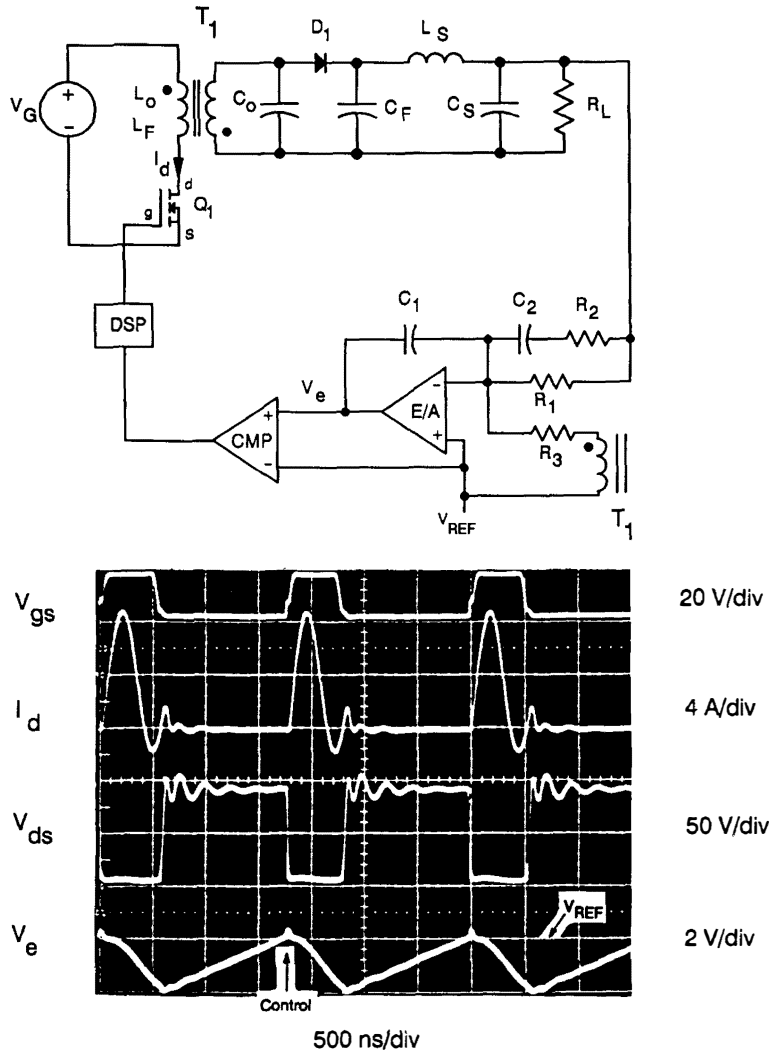

Fig. 14. Circuit diagram and measured waveforms of 1-MHz CSFM-controlled flyback QRC.

of CSFM control for a 1-MHz ZCS flyback QRC. Details of this circuit operation and design are presented in [8]. The resonant elements of the circuit are the transformer leakage, L_0, and secondary capacitor, C_0. The output capacitor of the flyback stage, C_1, is followed by a second filter to reduce switching ripple and noise. A secondary sense winding is added to the transformer core to provide inductor-voltage feedback which is then integrated through the amplifier to give the required cur-

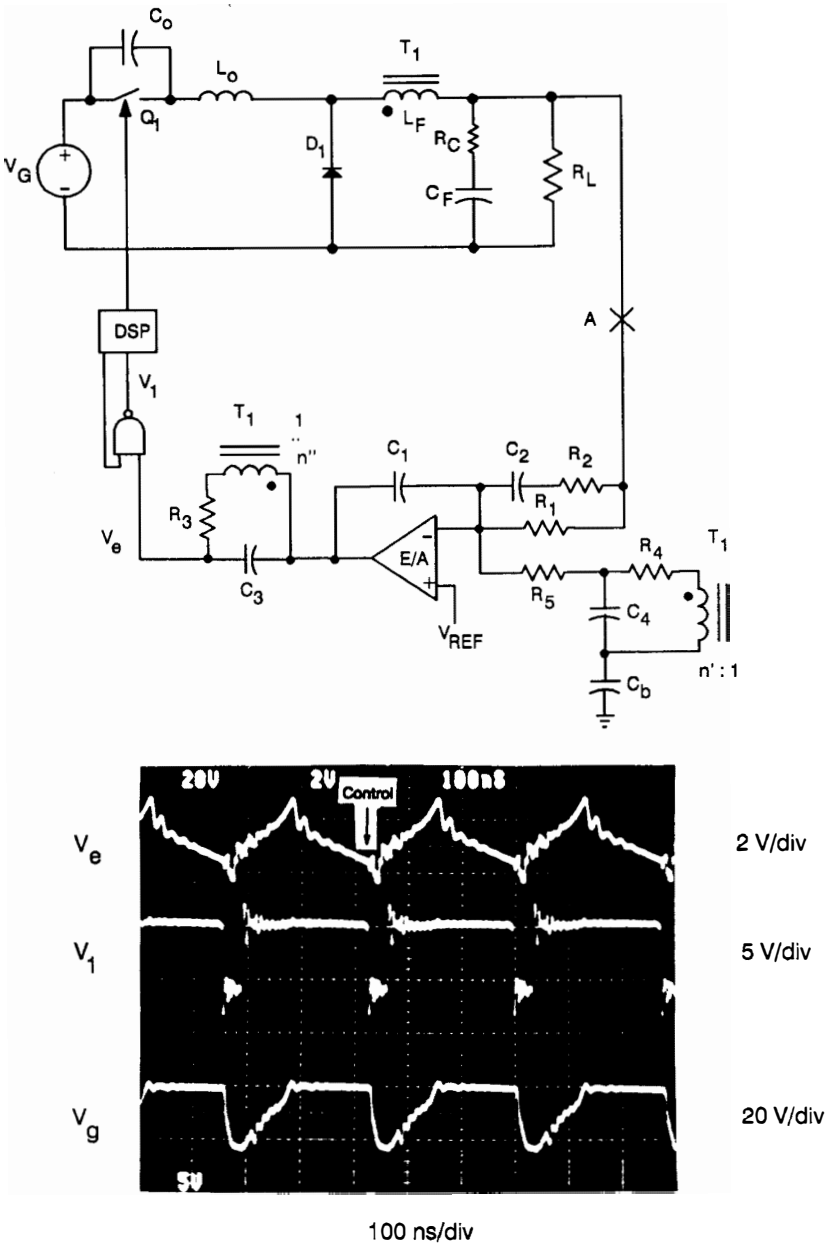

Fig. 15. Circuit diagram and measured waveforms of 7-MHz ZVS buck QRC with two-loop current sensing control circuit.

rent feedback for CSFM. The circuit waveforms of the converter are shown in Fig. 14. It can be seen that clean control signals can be obtained at 1 MHz using this scheme. Small-signal measurements of closed-loop audio susceptibility, output impedance and loop gain are presented in [8].

An LM360 comparator (National Semiconductor), a 74LS123 timer, and a DS0026 driver (National) were used in the logic and gate driver of the circuit of Fig. 14. The delay from the input of the comparator to the output of the DS0026 driver was too long for the circuit to be used at frequencies above 2 MHz. At higher switching frequencies, the control circuit described below should be used to improve performance.

B. 7-MHz Buck ZVS QRC

A ZVS buck QRC was built to show the effectiveness of the high-frequency control circuit which uses a passive network to generate the control ramp. The converter operated from a 12–20 V input, delivering 7.5-V output at 25 W. The minimum switching frequency at low line and full load was 4 MHz. At high line and light load, the switching frequency was 7 MHz. The circuit diagram and waveforms for this converter with control are shown in Fig. 15. The complete logic control circuit is very simple, consisting of an operational amplifier, four 74AC00 logic gates, and passive components. Details of the

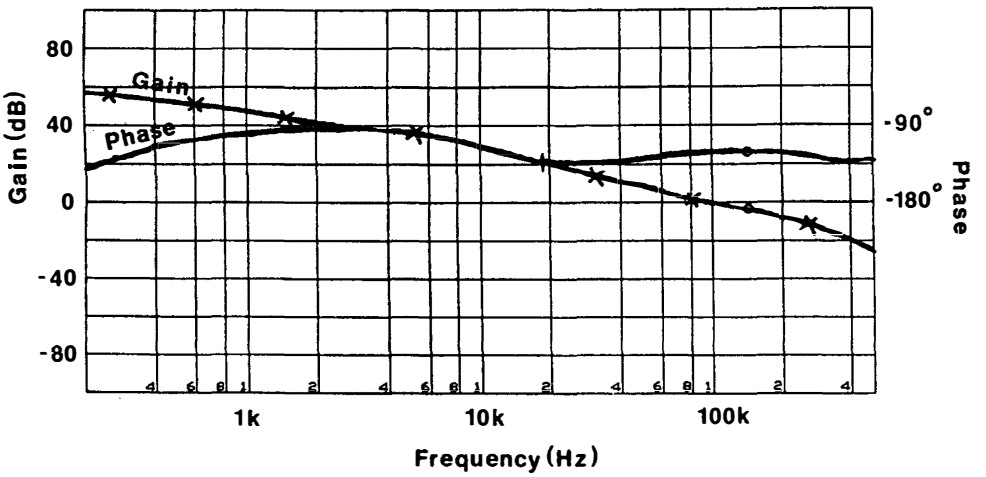

Fig. 16. Outer loop-gain measurement of 7-MHz ZVS buck converter.

complete circuit are provided in [9]. The comparator function after the error signal, V_E, was also implemented with a 74AC00 logic gate, since speed was critical and the threshold level of the comparator is not important. The total propagation delay from the thresold intersection to the fall of the current in the power switch is less than 20 ns, making this logic usable at switching frequencies up to 10 MHz. A clean control ramp was obtained at all switching frequencies. The relationship between the control ramp and the switching of the power MOSFET clearly shows the fast switching speeds achieved with the logic circuit.

Loop gain measurements were performed to verify the effectiveness of the control circuit. Several loop gains are formed by the CSFM control, but the only one that can be practically measured on the high-frequency circuit is that at Point A in Fig. 15. This loop gain shows the compensation-output transfer function with the current loops closed. The necessarily tight layout of the control-ramp circuit makes the current-loop gain extremely difficult to measure with any conventional techniques.

Standard loop-gain measurement techniques were used. A Hewlett Packard 4194A impedance/gain-phase analyzer was used to inject a sinusoidal disturbance into the loop and measure the input and output signals. Great care had to be taken to extend the loop-gain measurement range up to 1 MHz. Injected and return signals couple through unshielded circuitry and cables and make measurements invalid at higher modulation frequencies. Coaxial cables used to inject and measure the test signals were shielded with 5-mil copper foil, which was wrapped around the cables and grounded at the circuit. The cables were soldered directly onto the test points of the circuit with minimum wire lengths (about 3 mm). With this setup, good measurements were obtained up to 1 MHz. Beyond 1 MHz, noise coupling between the channels of the network analyzer affected the measurements. More care with grounding and shielding is required to extend the measurement frequency range further.

The outer-loop gain of the converter, shown in Fig. 16, has a crossover frequency of 100 kHz and a 60° phase margin. The phase of the loop gain remains well above −180° beyond 500 kHz. Theoretically, it should be possible to push the crossover frequency up to 500 kHz without instability. However, as the gain required of the amplifier increases, further phase delay occurs due to the gain characteristics of the amplifier. Fig. 17 shows the loop for the same circuit with a voltage compensation network which has decreased input impedance. (Referring to Fig. 15, components R_1 and R_2 are decreased, and C_2 is increased.) With an ideal amplifier, the phase would be identical to the previous measurement and the gain would be increased. The crossover frequency was increased to 180 kHz, but the phase margin at the frequency decreased by 20°. With this compensation network, gain required from the operational amplifier at high frequencies is 20 dB. Fig. 9 shows the intersection of a flat 20-dB gain with the gain characteristics of the amplifier. The two lines intersect at about 300 kHz, producing an additional pole at this frequency.

Further increase in loop-gain crossover can only be increased with an improved amplifier, or by cascading the amplifier with a dc gain stage having high bandwidth. With these techniques, it should be feasible to increase the loop-gain crossover frequency close to 1 MHz.

VIII. Conclusion

A new, multi-loop control scheme has been developed for ZCS or ZVS QRC's, providing a rugged system with excellent transient response and clean control waveforms. The VCO, which can be difficult to implement at higher frequencies, is replaced with a comparator.

The new control scheme, analogous to current-mode control for PWM converters, offers all of the small-signal benefits expected from current-mode control. The control-to-output, audio-susceptibility and output impedance transfer functions all have first-order characteristics at frequencies well below the crossover of the current loop. The voltage compensation is, therefore, much simpler to design and optimize for a desired closed-loop performance and the system is quite insensitive to power stage parameter variations.

A circuit implementation has been presented that allows multi-loop control to be used on circuits switching up to 10 MHz. This circuit requires few components and produces clean

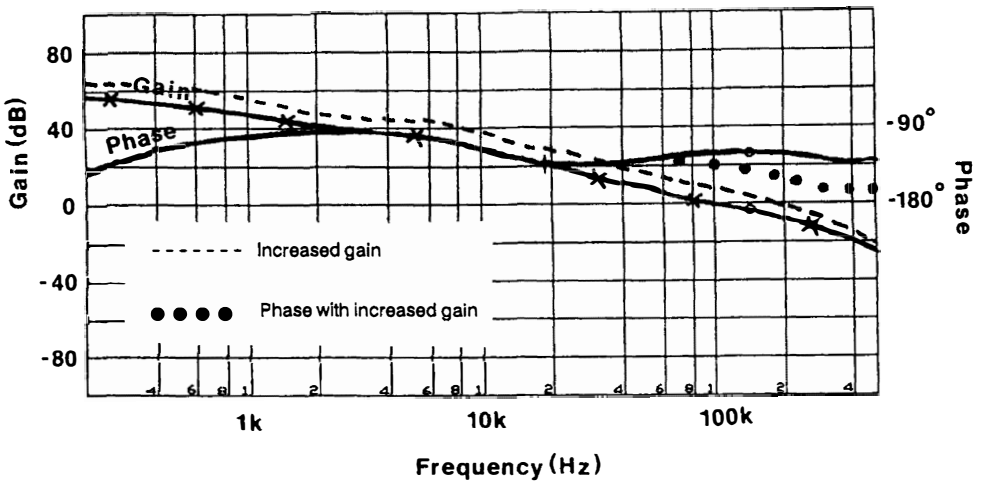

Fig. 17. Outer loop-gain measurement of 7-MHz ZVS buck converter showing band-width limitation of LF356 amplifier.

control waveforms. The application of this circuit has been demonstrated on a 7-MHz, ZVS buck QRC.

Good small-signal characteristics are obtained with this new control circuit. The cross-over frequency of the loop gain is limited only by the choice of operational amplifier. With this control scheme, it is possible to push the loop-gain crossover frequency beyond 1 MHz for a 5–10 MHz converter. This increase in crossover can significantly affect the size of the power-stage components, especially the output filter capacitor, which is usually determined in high frequency converters by the transient response requirement.

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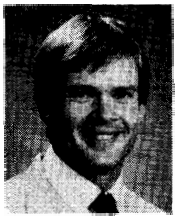

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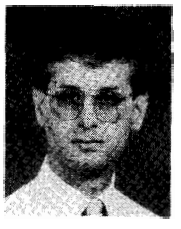

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Dr. Vorpérian has published 11 papers and is a member of Sigma Xi.

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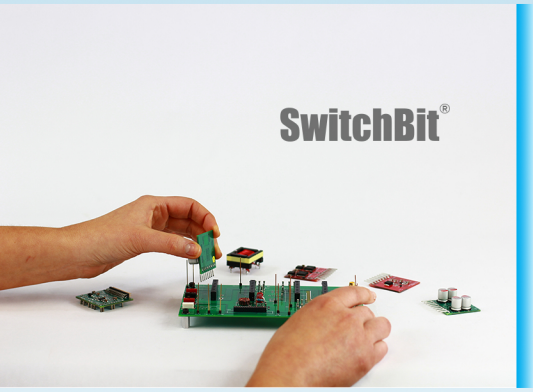

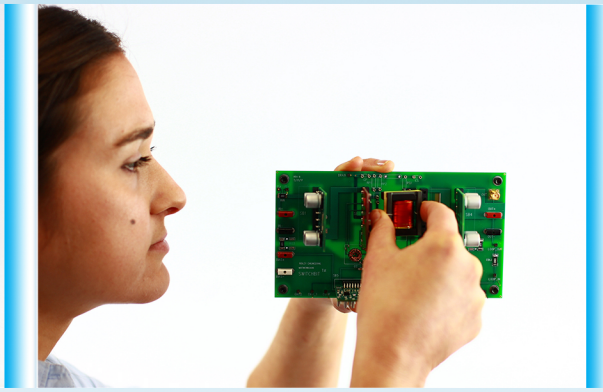

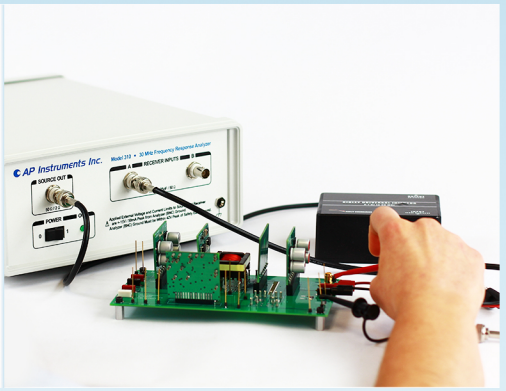

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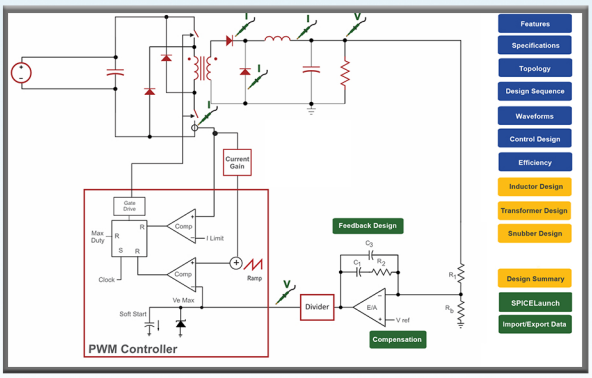

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