Analysis and Design of a Wide Input Range Power Factor Correction Circuit for Three-Phase Applications

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Abstract

A combined buck and boost topology power factor correction circuit which can operate with input voltages from 150 - 540 V is presented. The design and analysis of the operation and dominant losses of this circuit are given. The features of the topology are compared with those of a standard boost power factor correction circuit.

1. Introduction

Any power system which needs to provide more than 3 kW to the load is a candidate for three-phase input. Three-phase power input presents new challenges to designers of power systems which need active circuits to compensate for harmonic distortion and power factor. As with single-phase systems, there is a requirement from power users to have a single unit which will cover worldwide input ranges. For single-phase power, this translates into a voltage range from 85 V rms to 265 V rms, which covers low-line 120-V input to high-line 240-V input.

Three phase voltage ranges are from a nominal 208 V rms (line-to-line, no neutral is assumed) to a nominal 480 V rms. Low- and high-line variations provide a range from 150 V rms to 540 V rms. (This range can be higher in some countries - up to 600 V.) True three-phase rectifier circuits can be used for this application, but most of them are unable to handle a wide input range effectively. Three single-phase circuits connected across a three-phase system provide simple control, but the standard topologies used for single phase systems have problems with the input voltage range.

In this paper, a combined topology is presented which minimizes semiconductor stress, and provides an output voltage compatible with single-phase rectification technology.

2. Circuit Topologies

There are numerous three-phase topologies can be used, but most of them are unable to deal with wide input voltage ranges efficiently.

Fig. 1 shows conventional buck, boost, and buck-boost topologies for three phase power factor correction. The operation of these circuit is presented and analyzed in detail in [1]. Each of these topologies can offer the following features:

1) Sinusoidal input current
2) High-frequency switching harmonics *only* on input and output
3) No line-frequency harmonics with balanced input lines
4) Small filter components

However, the power switches of the three-phase circuits must be properly controlled to achieve these benefits, and this usually results in a microprocessor controller to generate the switch drive signals [1].

Furthermore, the operation of these circuits is complicated by the presence of unbalanced input voltage lines, a situation which is commonly encountered.

A. Three-Phase Buck Circuit

In addition to the above drawbacks, the buck circuit also suffers from the fact that the output voltage must be lower than the minimum of the input voltage lines. For a nominal 208 V input, this corresponds to about a 200 V dc output under worst case conditions of low line. The currents in the circuit under all conditions are then extremely high.

For example, for a 10-kW buck converter, the inductor current is continuously 50 A. Even at an input line of 480 V, when the filtered peak line currents are only 17 A, the switches continue to switch 50 A, albeit with a smaller duty cycle. Such operation is inefficient.

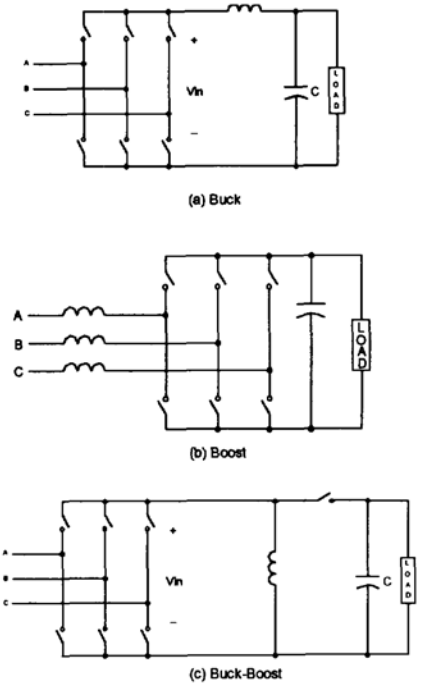


Fig. 1: Three-Phase Rectification Topologies

B. Three-Phase Boost Circuit

The three-phase boost circuit shown in Fig. 1b is the most common implementation of three-phase PFC, used for motor drives and many other high power applications. This implementation is very efficient and useful for narrow input voltage ranges. Over a wide input voltage range, the converter is less practical; the output voltage has to be higher than the peak line-to-line voltage rating (763 V), requiring a large step up from the boost switch at low line, and correspondingly low efficiency.

The high output voltage is also a problem for most dc-dc converter circuits. MOSFETs are optimized for operation in the 400-450 V range, and electrolytic capacitors provide excellent energy storage density for this voltage.

The high voltage problem can be solved with a pair of dc-dc converters in series at the output of the boost power stage, as shown in Fig. 2. This circuit requires balancing of the halves of the output voltage of the boost circuit, and careful consideration of the safety aspects of the system and failure modes. The efficiency problem still exists for low line operation.

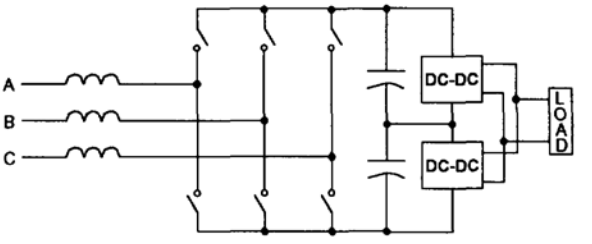


Fig. 2: Three-Phase Boost Circuit with Voltage-Sharing Loads

C. Three-Phase Buck-Boost Circuit

A standard buck-boost circuit, shown in Fig. 1c, can also be used for the three-phase power factor correction, but the drawbacks of a buck-boost in a dc-dc application are also relevant here. The input and output currents are both pulsating, and the switch sees a steady-state current larger than the input or output currents, and a steady-state voltage equal to the sum of the input and output voltages.

The buck-boost converter lends itself naturally to isolation, but the switch stresses make it impractical for high power operation.

D. Single-Phase Boost Circuits

The boost power factor correction circuit is the overwhelmingly most popular choice for power factor correction for single-phase applications [2]. When dealing with the lower voltages of single-phase input and a single input line, the output voltage of the boost is ideal for further processing, and the control circuit is very simple [3].

Three single-phase power factor correction circuits can also be used for a three-phase system, as shown in Fig. 3. Each converter requires an isolation stage, but this is not necessarily detrimental since it provides partitioning of the power into manageable size for higher-power applications.

For single-phase ac input, the dc bus generated by the power factor correction circuit is typically 350-400 V, and subsequent isolating power stages are usually optimized for this voltage level. However, in a three-phase, wide input range application, the use of three boost converters provides intermediate voltages of around 800 V. This presents complications in terms of device selection for the isolation

stage, transformer design and spacing, and choice of capacitors for energy storage.

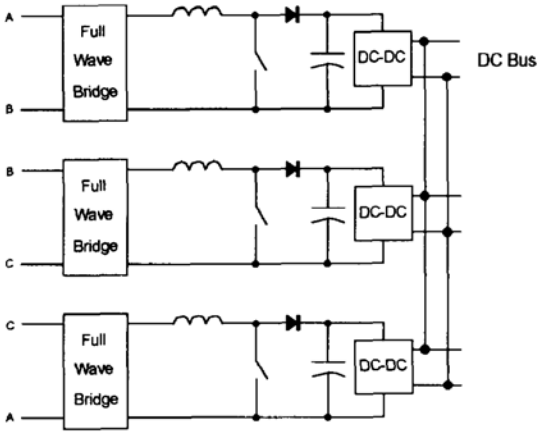


Fig. 3: Three Single-Phase Circuits used for Three-Phase Power Factor Correction

To reduce the output voltage of the converter, buck power stages could be used in place of the boost stages. However, the buck circuit can only operate when the input line is above the output voltage bus, and sinusoidal currents cannot be attained. Single-phase flyback circuits could also be used, but these suffer from pulsating currents and high switch stress, as discussed earlier.

3. Buck + Boost Circuit Topology

A better way to provide single-phase power factor correction is to use a combination buck and boost converter, as shown in Fig. 4. This circuit has been proposed before [4], operating on the verge of discontinuous mode. For high-power operation, this is inefficient, and the circuit should be run in continuous conduction mode to minimize conduction losses.

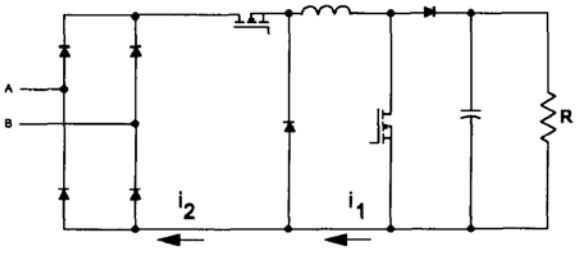


Fig. 4: Buck + Boost Topology with Compound Buck Switch for Maximum Efficiency

It is important to realize that the power switches in the new circuit are not operated with the same duty cycle. (This would result in buck-boost or flyback operation, which would significantly increase circulating currents, switching loss, and conduction loss.) Instead, the buck switch is closed continuously when the input line is below the output voltage, and the circuit is operated as a normal boost converter in this region. When the input line is above the output voltage, the boost switch is open, and the buck converter operates.

At low-line input, the circuit operates as a normal boost converter for maximum efficiency, and the corresponding circuit waveforms are shown in Fig. 5. As the input line is increased, the buck circuit operates at the peak of the line, and the circuit waveforms for high line are shown in Fig. 6.

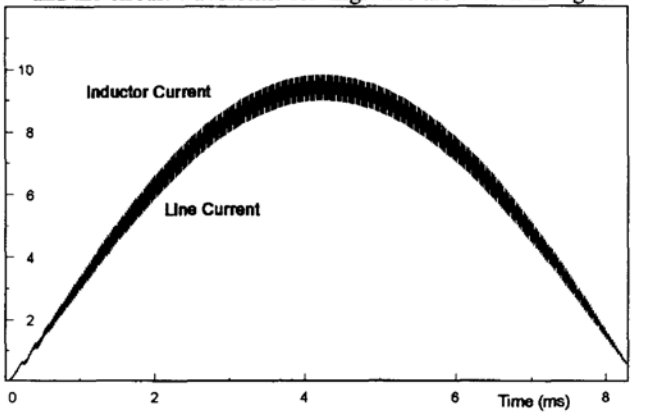


Fig. 5: Buck + Boost Current Waveforms At Low-Line Input (Buck Stage Inactive)

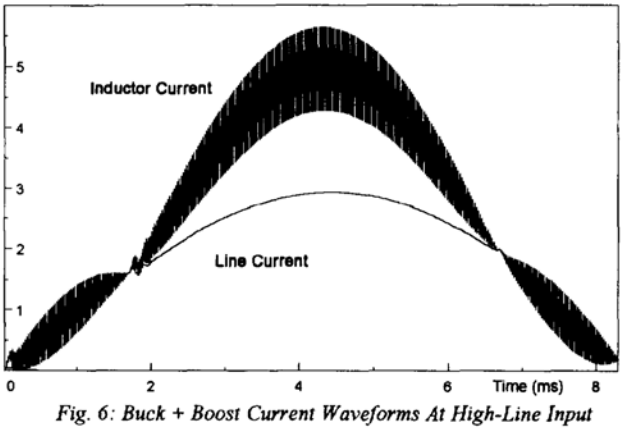


Fig. 6: Buck + Boost Current Waveforms At High-Line Input

The combination buck + boost operation allows the output voltage to be regulated at any desired level. The choice of output voltage is determined by efficiency characteristics, discussed in the next section, and by compatibility with existing dc-dc converters. A 350-400 V level for the output

voltage provides compatibility with existing single-phase system hardware.

4. Switch Conduction Loss Analysis

A significant problem when trying to use a standard boost converter for wide range input voltages is loss of efficiency at low-line input. The large step-up needed to produce the high output voltage from low-line input results in a large duty cycle of the power switch. The switch conduction loss for a normal boost converter [5], neglecting ripple current in the power switch is given by:

$$P^{bst} = \frac{4P^2R}{V_p^2}\left[\frac{1}{2} - \frac{4V_p}{3\pi V_o}\right] \quad (1)$$

Where P is the output power, V_p is the peak of the input line voltage, V_o is the output bus voltage, and R is the on-resistance of the boost FET. At low input voltages, where the peak input voltage is much lower than the output voltage, the conduction losses increase rapidly with the inverse square of the input voltage.

The conduction losses for a normal boost converter operating with an 800-V bus are shown in Fig. 7 for a 1.5-Ohm, 1000-V device. These results show that the boost switch alone cannot be better than 95% efficient at low line, neglecting any switching losses.

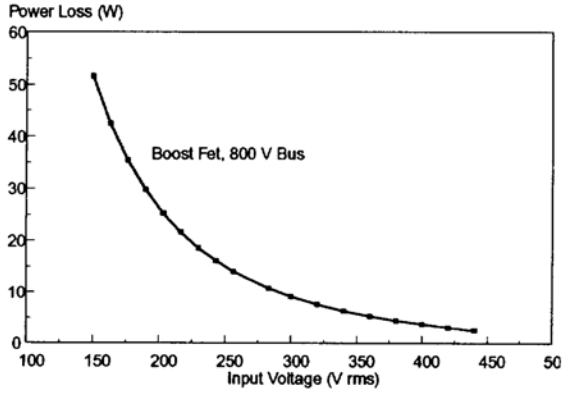


Fig 7: Power FET Losses for a Boost Converter with an 800-V Bus

Switch conduction losses decrease rapidly with increasing input voltage. The best efficiency is obtained when the output voltage is just above the peak input voltage, and the boost switch is operating for a minimum amount of time.

The buck + boost converter can improve this low-line efficiency by providing a lower output voltage bus, and requiring a smaller step-up. When operating in buck + boost mode, the conduction loss of the buck power switch during the buck cycle of operation can be expressed as:

$$P^{bck} = \frac{8P^2R}{\pi V_p V_o}\int_{\arcsin\left(\frac{V_o}{V_p}\right)}^{\pi/2} \sin^3 t\,dt \quad (2)$$

During the buck + boost operation, there is also some loss due to the boost region of operation at the beginning and end of the cycle. This is given by:

$$P^{bst} = \frac{8P^2R}{\pi V_p^2}\int_0^{\arcsin\left(\frac{V_o}{V_p}\right)} \sin^2 t\left[1 - \frac{V_p}{V_o}\sin t\right]dt \quad (3)$$

Finally, there is some loss during the boost region of operation when the buck switch is always on. For the most efficient operation, a bipolar device is used in parallel with the FET during this region to minimize conduction losses. A slow device can be used here since it only turns on and off once every half line cycle. This device is often used also with a boost converter to control inrush current and voltage surges. The losses associated with this device, assuming a constant voltage drop, are given by:

$$P_{aux}^{bck} = \frac{4PV_{ce}^{sat}}{\pi V_p}\left[1 - \sqrt{1 - \frac{V_p^2}{V_o^2}}\right] \quad (4)$$

Fig. 8 shows the FET and bipolar conduction losses for a 1-kW buck + boost PFC circuit. A 1-Ohm, 500-V device is assumed for the boost FET, and a 3-Ohm, 1000-V device for the buck FET. (Similar silicon area was used for this circuit as for the boost converter of Fig. 7.) A 2-V drop was assumed for the bipolar device. Fig. 9 shows a comparison of total switch conduction losses for the new converter circuit, and for a boost converter with a series bipolar device for inrush limiting and surge protection in case of an input line transient. At low-line, the buck + boost converter offers a substantial efficiency improvement. The normal boost converter must produce an 800-V bus, and the duty cycle of the power switch is much longer than the buck + boost converter with a 400-V bus.

The overall system efficiency using the two converters will also be impacted by the different output voltages, and choice of components for a dc-dc converter designed for 400 V versus 800 V.

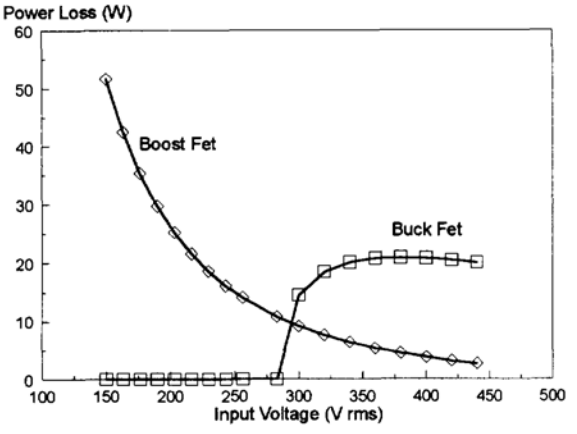


Fig 8: Power Switch Conduction Losses for the Buck + Boost Converter with a 400-V Bus

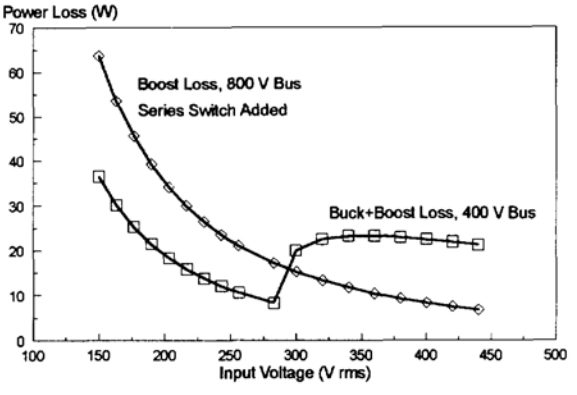


Fig. 9: Comparison of Total Conduction Losses for a Boost Converter with Surge Protection Switch and Buck+Boost Converter with Inherent Surge Protection.

5. Input Line Failure Redundancy

An important consideration for three-phase power inputs is the ruggedness of the system under abnormal line conditions. Single phase systems usually need to consider the cases of extreme voltage range for relatively long durations (i.e. ten or more input line cycles), and voltage dropouts for short durations (one or two input line cycles).

Other abnormalities can exist in three phase circuits. In addition to low and high voltage extremes, it is possible for a single input line to fail completely, either in an open or closed condition. When this happens, a source of input power is still provided by the remaining two input lines.

A normal three-phase bridge rectifier will ride through such an event automatically. The remaining line-to-line voltage is rectified as for a single phase system, merely causing greater ripple on the output voltage bus. Output power can be maintained as long as the breakers on the remaining lines do not trip.

In implementing power factor correction for three-phase systems, it is important to maintain this ruggedness. Under a line-open failure, the system of Fig. 3 will only have one converter which has power available at its input. In order to process the full load current, each of the modules of this system would have to be three times oversized.

This line-failure problem is simple to overcome with the circuit of Fig. 10 [6]. The addition of SCRs to the input of each line converter provides a connection to the additional input line when an undervoltage is detected on the input phase to the converter.

This circuit allows complete redundancy in the case of an input line failure, with no oversizing of the power components. Each circuit will share one third of the line current under failure conditions, providing that the final dc-dc converters are current-regulated. Notice that unity power factor is also maintained for the remaining input line.

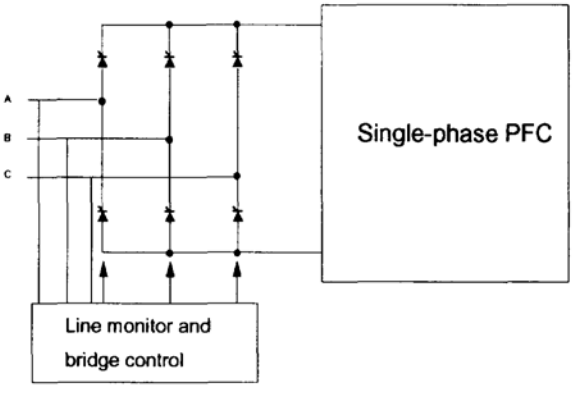


Fig. 10: Circuit for Implementing Line-Failure Redundancy

6. Control Circuit Implementation

Another important aspect of the buck and boost power factor correction circuit is the control network. It is necessary to have a rugged control circuit which is stable under all conditions of line and load, and which can provide low line-current distortion over as wide a range as possible.

The single-phase boost circuit can be controlled with a single integrated circuit which provides a PWM ramp, feedback compensators for the output voltage feedback and line current feedback, and a multiplier for generating a reference sine wave from the input voltage line and the error voltage [3].

This control circuit is suitable for a boost converter operating over a wide input voltage range. The small-signal gain of the boost circuit is a function of the output voltage of the converter, which is constant, so it is easy to optimize the circuit for the whole line range of operation.

The buck converter, however, has a small-signal gain which is a function of the input voltage to the converter, which changes considerably for this application. As discussed in [7], a wide current-loop bandwidth is necessary to maintain low line distortion, and this can be difficult to achieve with a changing power stage gain.

The circuit shown in Fig. 11 can be use for controlling the buck and boost power factor correction circuit [8]. This circuit consists of two PWM ramps, one for each of the power switches (buck and boost switches). The upper ramp, offset by a dc voltage, controls the duty cycle of the boost converter, and has a fixed offset voltage and amplitude, corresponding to the fixed power stage gain of the boost converter.

The lower ramp, starting from zero volts, is used to control the buck power switch. The amplitude of this ramp is proportional to the input voltage to the buck switch. This provides feedforward of the input voltage to the control of the duty cycle, reducing the distortion arising from steady-state errors in the control circuit at line-harmonic frequencies. The variable ramp also cancels the changing gain for the power stage, allowing a higher bandwidth loop to be designed for feedback of the inductor current.

Two current-feedback loops are used in order to provide adaptability to changing power stage operation and to minimize the distortion of the input current waveform. In each of the current feedback amplifiers is a network to provide a true amplification of the difference of the current signal and the error reference signal, again in order to minimize distortion. This is shown in Fig. 11b. Four operational amplifiers are needed to implement this function for both of the current feedback loops.

This control implementation provides a compromise between the complexity of a microprocessor design which could eliminate almost all distortion, and the simplicity and ruggedness of the single-chip solution for single-phase power factor correction circuits.

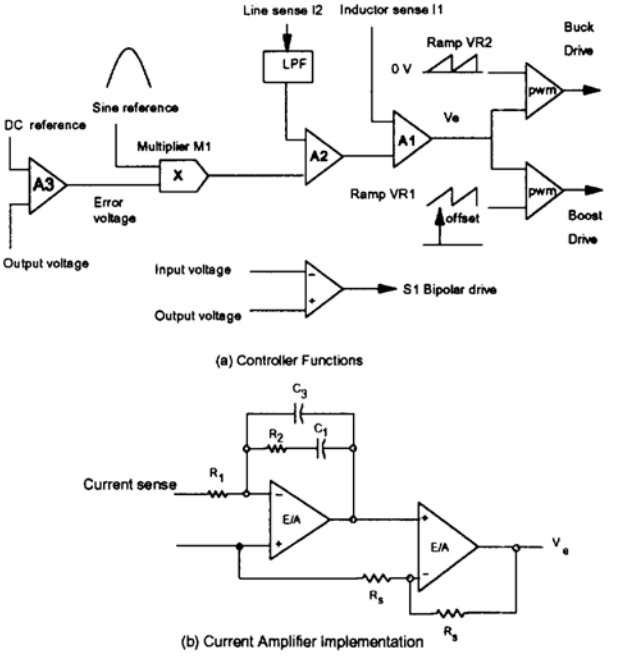


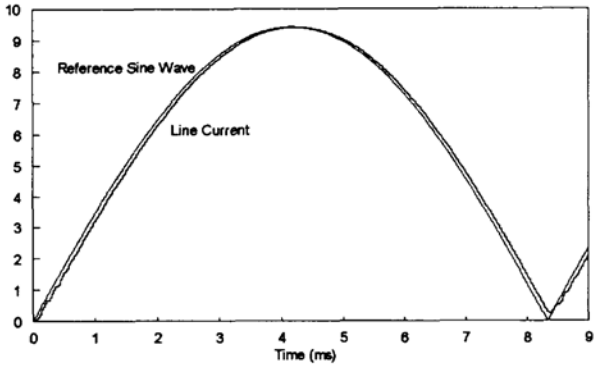
Fig. 11: Control Circuit for Wide-Range Stability and Low Line-Current Distortion

7. Simulated Results

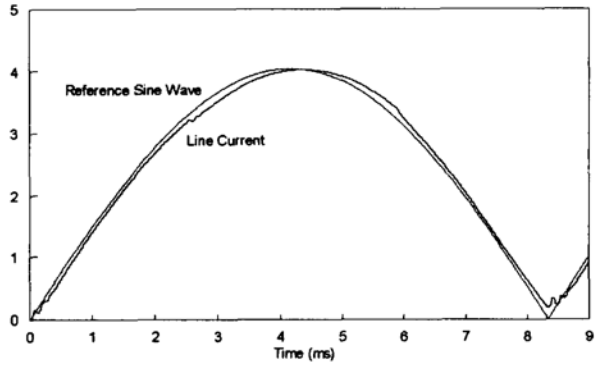
Experimental results for distortion and efficiency measurements are still in the preliminary stages. However, the operation of the circuit described in this paper has been tested thoroughly through computer simulations. In order to effectively simulate the 600 cycles of switching operation needed to show the waveforms and distortion, simulation speed-up techniques described in [9] were used.

The circuit to be simulated was designed for 1-kW output power, and a switching frequency of 50 kHz. The converter was designed to operate from 150-540 VAC steady-state conditions.

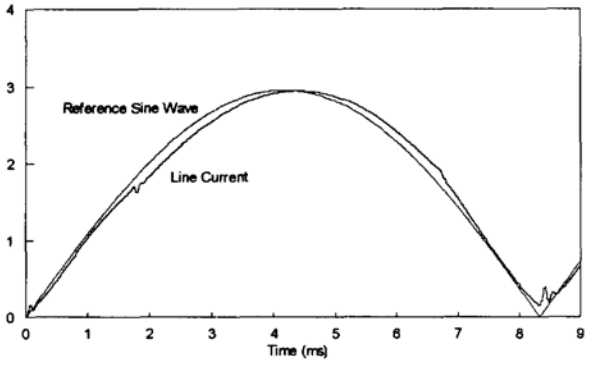
The current distortion is very low for boost-mode operation. The dual current loops of the controller reduce distortion arising from steady state errors considerably when compared to a conventional boost power factor controller. At higher line and lighter load, the line current distortion increases. Further optimization of the controller is expected to provide a total harmonic distortion of less than five percent.



(a) 150 V Input, 1-kW Output



b) 350 V Input, 1-kW Output



(c) 480 V Input, 1-kW Output

Fig. 12: Circuit Waveforms for Different Input Lines.

8. Conclusions

A new converter suitable for wide-range input voltages has been presented. The combination buck and boost converter is capable of regulating an arbitrary output voltage, while maintaining close to unity power factor. This can save considerable development time since standard dc-dc converters developed for single-phase applications can continue to be used at the output of the power factor correction circuit.

The operation and switch conduction analysis of a wide-range input converter has been presented. Low-line efficiency is much improved compared to a standard boost. Worst-case switch dissipation is considerably lower than that of a boost converter designed for the same application with a higher output voltage bus.

A simple circuit can be used to provide system operation in the event of a single line failure, and unity power factor can be maintained indefinitely under these conditions. This is achieved without having to oversize any part of the power system, resulting in considerable savings.

References

1. K. Ngo, *"Topology and Analysis in PWM Inversion, Rectification and Cycloconversion"*, PhD Dissertation, Power Electronics Group, California Institute of Technology, May 1984.
2. M. Kocher, R. Steigerwald, *"An ac-to-dc Converter with High Quality Input Waveforms"*, Power Electronics Specialists' Conference (PESC '86) proceedings, 1986, pp. 531-540.
3. L. Dixon, *"High Power Factor Preregulators for Off-Line Power Supplies"*, Unitrode Switching Regulated Power Supply Design Seminar Manual, SEM-700, 1990.
4. E.G. Schmidtner, P.W. Busch, *"Off-Line Power Supply with Sinusoidal Input Current and an Active Limit to the Inrush Current"*, Power Conversion (PCIM) Conference Proceedings, Nurnberg, Germany, June 25-27, 1991.
5. Z. Chen, *"Design and Analysis of an Active Power Factor Correction Circuit"*, Master's thesis, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, September 1989.
6. R. Ridley, S. Kern, *"AC/DC Converter"*, Swiss Patent Application #00 991/92-9
7. Z. Chen, M Jovanovic, *"Design Trade-Offs in Continuous Current-Mode Controlled Boost Power Factor Correction Circuits"*, High-Frequency Power Conversion Conference (HFPC '92), 1992.
8. R. Ridley, S. Kern, B. Fuld, *"A New Control Circuit for Wide-Range AC-DC Converter"*, Swiss Patent Application.
9. R. Ridley, *"New Simulation Techniques for PWM Converters"*, IEEE Applied Power Electronics Conference (APEC '93), 1993.