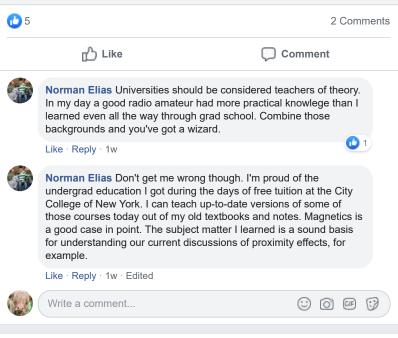
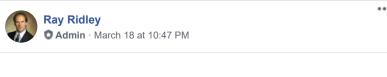


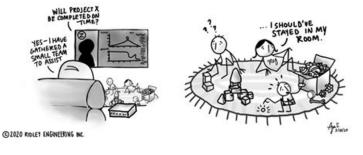


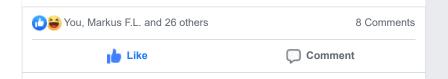
Tapping Essentials - Every Machinist Needs to Watch This -**Haas Automation Tip of the Day** 





## OHM CONFINEMENT WEEK 2 - SCHOOL'S CANCELLED





Like · Reply · 1w



David Edwards # Ray Ridley, what happens now? Should I expect to receive a product key and download link via email? No hurry, just wondering.















Figure 1 - Available Schematic.

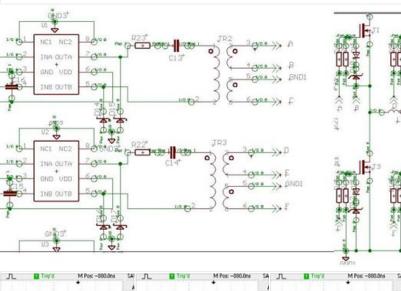
Figure 2 - The signal's of the Secondary's of the gate drive transformer. ( without the mosfet )  $\,$ 

Figure 3 - The signal When I put a 500R resistor between the secondary's. ( without the mosfet )  $\,$ 

Figure 4 - The signal of the secondary when i add the mosfet.

Where is the mistake, where am i doing wrong?

Thank you in advance!







30 Comments



Comment



Jeremy Lister C13,C14 value?

Like · Reply · 2w



Mikail Ünal 🚂 1uF

Like · Reply · 2w



**Ishrat Jamal** Mikail Ünal pulse transformer design and measurement details? Ex. Inductance.

Put c13 and c 14 close to 100nF. This cap is just to avoid DC component going to primary of the pulse transformers.

Like · Reply · 2w



Alex Berestov Leakage inductance.

Like · Reply · 2w



Mikail Ünal So what should be the average value to drive of the leakage?

or does it have a numerical value?

way to couple windings better without compromising isolation. That usually means smaller distance between pri and sec and more or less regular winding.

b) Measure it with LRC meter.

c) Fr=1/sqrt(L\*C). So if you know gate capacitance you can figure out Ls. But you need to find resonance frequency.

Like · Reply · 2w · Edited



Yuri de Klerk R22, R23 value?

Like · Reply · 2w



Mikail Ünal W Yuri de Klerk 30hm's

Like · Reply · 2w



Ray Ridley there are a lot of missing component values.

back to back zeners are the norm - you have a diode and a zener.

Like · Reply · 2w



Ray Ridley 🔮 transformer design is key. You can't just grab any transformer off the shelf.

half the schottky clamps are missing on the drive pins.

Where did this design schematic come from?

Like · Reply · 2w



Mikail Ünal Ray Ridley i did this take from ucc28950's datasheet also there are too many design's with this circuitry but it's true that i've take it from the grab:)

Like · Reply · 2w



Riccardo Tinivella Did you try with a capacitive load also? Cgs+Cgd with miller effect loads the drivers capacitive

Like · Reply · 2w



James Keith May be this can help you. I found this from TI's reference board schematic ( 600 W PSFB design )



Like · Reply · 2w · Edited



Mikail Ünal P Thank you sır, do you know what the LL, Hipot means?

Like · Reply · 2w · Edited



Roswell Bob LaFrank I have used binocular cores well into MHz region

Like · Reply · 2w · Edited

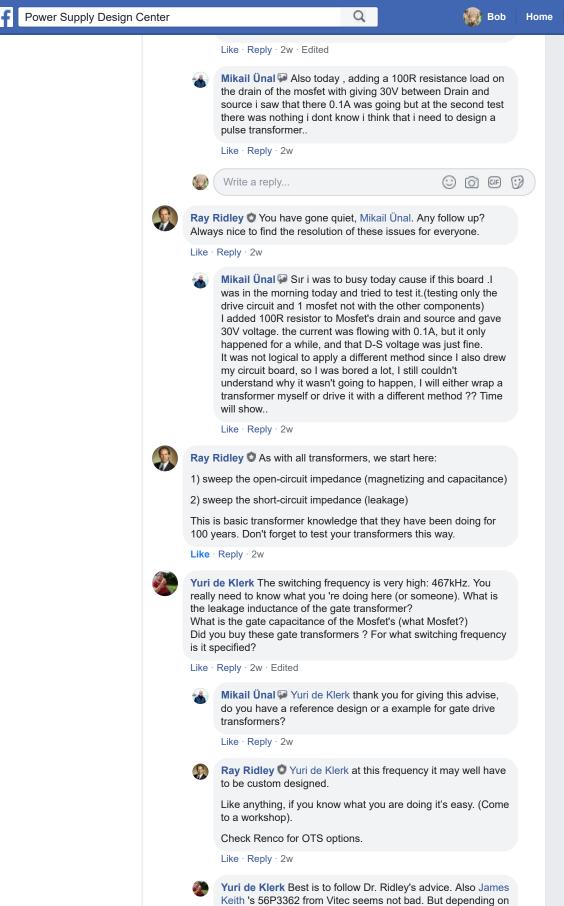


Roswell Bob LaFrank There is no mistake. These waveforms are exactly what you should expect given the loads that you are driving. You have a resonant gate drive circuit. The reactance of the transformer is playing with the capacitance of the mosfet to give you a nice sinewave. You should be looking at a lower inductance transformer design if it bothers you. I am basically repeating what Alex Berestov said with two words.

Like · Reply · 2w · Edited



Bob Gudgel I was thinking that it was resonant also. I normally add capacitive coupling to the secondary and then diodes/zeners at the G-S of the FET



the size of Mosfet's you might need additional circuitry to drive

(I) (II) (II)

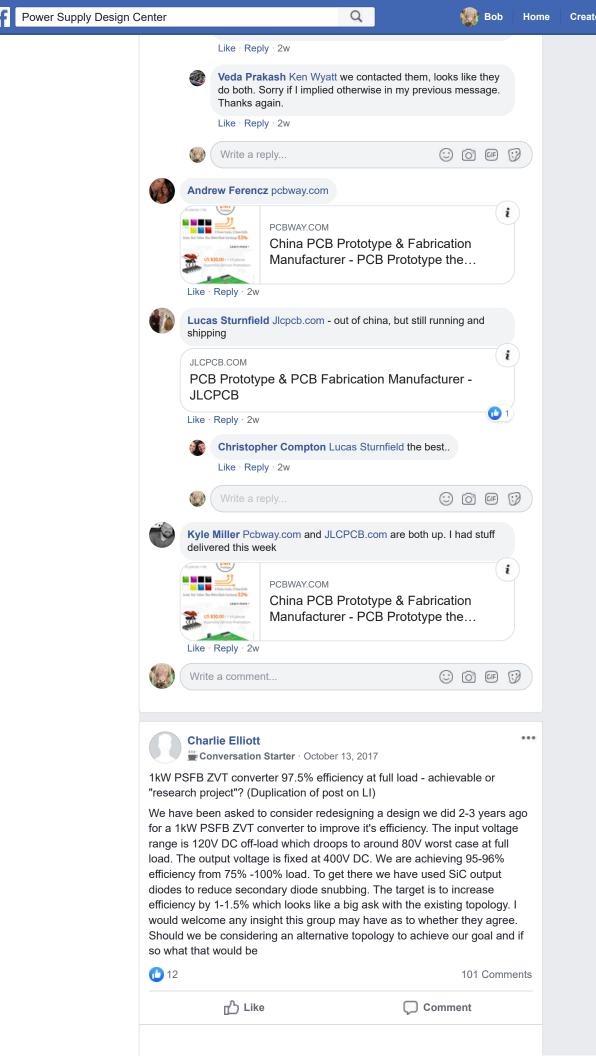
them.

Like · Reply · 2w

Write a reply...

**Ken Wyatt** Veda Prakash sorry, thought his shop did both.

Like · Reply · 2w



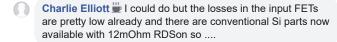
Existing system is full bridge output diodes with 200V 20mOhm TO220 Fets on the inputs, ETD59 transformer using the leakage as the "resonant" inductance and sendust output choke. 30kHz operation for a combination of reasons but this could change if required. I am quite space constrained. LLC has of course been

suggested!! Like · Reply · 2y



## Casper Hjort Wilson GaN FETs?

Like · Reply · 2y

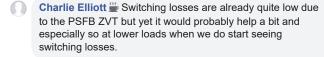


Like · Reply · 2y



Casper Hjort Wilson Lower switching losses..?

Like · Reply · 2y



Like · Reply · 2y



Write a reply...









Colin Tuck Well, where are the losses currently? Tx? o/p diodes still? housekeeping circuitry and assoc psu? this info is paramount to intelligent loss reduction...

Like · Reply · 2y

Hide 16 Replies

Charlie Elliott 
Despite using SiC output diodes, we still have appreciable snubbing losses - around 8W. The SiC diodes themselves almost doubled the conduction losses vs the original Si diodes but it was an overall improvement due to significant drop in snubbing. Losses in the 4 SiC diodes are around 10W. The transformer is also going to get a good revisit as I suspect that there is more AC loss in the windings that there should be. We are using foil for the primary at the moment resulting in more "layers" than I would like. There is a bit of history there as the customer spec has changed many times. Originally this was full power at 40V design.

Like · Reply · 2y



Colin Tuck Oh kay, you need slower transitions on the switching edges to reduce the hit on the diodes, thus caps across the fets ~ 10nF or bigger, and suitably sized series L on the Ph shift full bridge, with perhaps a gap in the Tx to increase energy storage for the transitions here too...

Like · Reply · 2y



Colin Tuck Fet turn off, as seen at the gate should be 12V to 0v in <40nS to get mostly lossless turn off...

Like · Reply · 2y



Colin Tuck IN PhSFB the pri current is always in the Tx so the Cu has to be sized for this...

overcome by having a 1:20 tap on the o/p choke, the B-rect goes to the tap, a diode goes from the LHS (close to tap) to gnd (anode to gnd) and the RHS of the choke goes to the filter cap, this way when the Tx is shorted by the bridge the o/p current flows only in the o/p choke and one diode only (the added one) the rectifying diodes are slightly reversed biased, aiding (reducing) switching losses for the next power pulse...

Like · Reply · 2y

Colin Tuck I'm pretty sure Colonel MClyman invented this very useful technique ...

Like · Reply · 2y

Charlie Elliott Colin Tuck - Agreed we should look at slowing the transitions again. In the past we have tested with added caps and additional resonant L but then turn off losses were killing us. However that was when we were down at 40V so certainly worth looking at again.

Like · Reply · 2y · Edited

Charlie Elliott Colin Tuck - The tapped output inductor idea sounds interesting. Certainly not looked at that before. I hope it isn't patented!!

Like · Reply · 2y

Cameron Stewart I would recommend replacing the copper foil with LITZ wire.

Like · Reply · 2y

Charlie Elliott Cameron Stewart - Yep already high on the list 😊

Like · Reply · 2y

Colin Tuck Not sure if it was ever patented - I suspect not been in public domain for >30 years I think ...

Like · Reply · 2y

Lotfi Bgh how much core losses do you have?

Like · Reply · 2y · Edited

Yurii Shynkarenko Colin Tuck I am agreed with Colin Tuck. Increasing diameter or sq.mm of the primary in twice will reduce copper losses. There is an additional current of a freewheeling period when the primary is shorted and heating. It is the main disadvantage of PSFB topology.

Like · Reply · 2y

Charlie Elliott "Yurii Shynkarenko - Changing from foil to litz on the primary will probably reduce losses overall due to reduction in AC component despite the poorer fill factor. However straight increasing the size of the wire on primary without looking at secondary as well isn;t a good idea I am sure you will agree. My transformer is already quite full.

Like · Reply · 2y

Charlie Elliott Lotfi Bgh - Calculations say core loss is about 5W at 100 deg. C taking into account the first few harmonics of flux.

Like · Reply · 2y

Lotfi Bgh If you don't mind increasing your core size, you can consider reducing the current ripple ratio. This way, you decrease the magnetic field swing and the core loss and also the coil AC loss. You will get higher DC loss though but maybe lower than the actual overall inductor loss.















Magnus Rosén Hmm ... indeed a great task. Efficiency from 95% to 97.5% mean to slash the losses by half. From 50W to 25W. Agree that its wise to start invedtigste the options where losses are pretty large. Tx, Rec and houskeeping (Sorry for not bringing any improvement idea for the time moment)

Like · Reply · 2y



Erhan Demirok you may consider to use synchronous rectification at the secondary with center-tapped xtr

Like · Reply · 2y



Dave Lafferty Can you use an active snubber to return some of the power back to the rails?

Like · Reply · 2y



Charlie Elliott Pay has already suggested that and I agree that it is a good idea to look at.

Like · Reply · 2y



Stephen Berry Nonlinear Coss with voltage can cause commutation problems in the PSFB. Consider other MOSFET options. Definitely dump the foil transformer primary it's capacitance and ac resistance will cause problems. Why did you use sendust for the output choke?

Like · Reply · 2y



Charlie Elliott PRe sendust, for packaging reasons we needed to use height but not PCB area which pushed me towards a toroid. Sendust met the cost and size requirements very nicely. There are lower loss solutions out there of course and it may be I need to revsit the output choke but it is a little way down the list.

Like · Reply · 2y



Cameron Stewart My thinking parallels Colin Tuck's in that you need to make a "power loss budget" for the entire converter.

That means coming up with accurate power dissipation numbers for your various switching and conduction losses for all your components (easier said than done) and then looking at what can be improved -spreadsheet wise - to meet your goal.

As far as LLC, another alternative is straight series resonant under phase shift full bridge control.

Like · Reply · 2y



Charlie Elliott # Hi Cameron, thanks for the reply. Series resonant under phase shift control is something I have never considered. Presumably it still requires an output inductor or am I missing something?

transformer and rectifiers directly drive the output capacitors with sinewave resonant current.

To be honest, I haven't done series resonant under phase shift control yet. When I have time, I want to build a Spice simulation to explore the concept.

The series resonant inductor runs HOT due to core loss from high AC flux. The primary peak currents are also much higher. Getting current limit and voltage regulation to work properly is a control problem not to be taken lightly. Unlike you, my approach implementation would use analog control rather

With a 200V winding and a voltage doubler on the output directly driving the capacitors, the diode snubbing problem would be eliminated. A full wave rectifier bridge using a 400V winding is also feasible.

Changing power stage topologies means a brand new development curve for both power and control. It's better to slightly tweak a design that already works when you can. A new power stage topology is something to consider when you have finally run out of maneuvering room with the existing approach.

Like · Reply · 2y · Edited



Cameron Stewart LLC has cost reduction advantages because you can use a half bridge rather than a full bridge. Again, the inductor is on the primary, delivering sinewave resonant current direct to the output capacitors from the transformer and rectifiers.

There are plenty of analog control chip solutions already in place. I don't know how well established digital control is with LLC. It sounds like a potential development headache without proven code already in hand. You are also at the upper end of power level or beyond for LLC at 1kW.

Like · Reply · 2y · Edited

Charlie Elliott Cameron Stewart - Re series resonant FB with phase shift and no output inductor, I just remembered that we inherited a 25kW system with that topology to try and fix a little while ago. The company who were developing it were struggling in many areas. My initial concern as to how well it could be controlled was sadly proved true. Even combining limited variable frequency modulation with phase shift control we could not achieve the required output voltage and load range required for the application (EV DC fast charge). As a result the project was canned. Never got the opportunity to investigate whether they just had the turns ratio and LC values / frequency wrong.

Like · Reply · 2y · Edited



Charlie Elliott Cameron - digital control for LLC doesn't worry me. Already have that developed and in many ways allows the kind of flexibility in control required to cover everything. You do have to make sure you have sufficient timing resolution of course especially on higher power systems or else 1 bit change can get scary!! Going for LLC will be a last resort as far as I am concerned as it will be a start from scratch. We will go after the low hanging fruit with PSFB with the existing PCB and control first and see where that takes us.

Like · Reply · 2y



Cameron Stewart With series resonant topologies: You need to get a working simulation first as proof of concept before you build hardware.

Turns ratio and input voltage range are critical with the series resonant topology. If the input voltage range varies by more than +/-10% it is prudent to use a pre-regulator in front, thereby impacting efficiency to achieve proper control.

Alex Berestov Series LC not mentioning LLC will deteriorate all other specs. However, filter starting with a capacitor and not the inductor will provide ZVS/ZCS at the rectifiers' diodes. That said the next logical step would be DAB. It's probably as complex as active non-dissipative snubbers with power recovery. But this means that Vicor's approach is even more complex: ZVS preregulator plus unregulated self-oscillating series LC with synchronization (some kind of PLL). Two stage conversion is not that uncommon and is widely used in AC-DC converters, especially at higher input voltage

CIF

Colin Tuck With say 200- 250nS transitions times, 50kHz should be an easy freq to operate at and not hit the diodes too hard, a Tx with layered litz should get the Tx losses down to under 4W total without too much difficulty - we get 4W for our 1.5kW PSFB at 48V out (385VDC in) in an ETD44 at 125kHz ( 3C96 ). Getting good low loss 1206 caps across the fets is the key, along with very strong pull down on the gate drive to eliminate turn off losses...

Like · Reply · 2y



Yurii Shynkarenko Hi Colin,

"4W losses for an ETD44 at 125kHz ( 3C96 )" - It's mean that a TX temperature is raised up to 80-90C degree if there is no fan. Am I right? What TX temperature did you get without a fan at full load?

Like · Reply · 2y · Edited



Colin Tuck We never measured the Tx temp without the fan running - sorry.

Like · Reply · 2y



Charlie Elliott Thanks everyone for you helpful comments and in particular Colin Tuck for the useful real-world reference points. As I was already aware and several of you have pointed out, ditching the foil in the transformer is probably priority 1. I will also consider a lift in frequency but need to look at the control as it is digital and I am concerned about timing resolution.

Like · Reply · 2y



Charlie Elliott # If I were to consider a resonant design, one concern I have is the cost and reliability of the capacitance required given the power and voltage. Rough calculations suggest the cap would carry around 20A. Would anybody have any recommendations for parts to consider?

expressiy designed for triis applicati

Like · Reply · 2y



Colin Tuck Don't give up on phase shift just yet ...! We design a lot of resonant converters, and yes the pri side caps need to carry large currents in your design, but a new lower leakage, lower loss Tx and slower transitions, should bump up your efficiency without massive engineering input...

Like · Reply · 2y



Charlie Elliott # I have certainly not given up on the PSFB. I would have to be very confident that an alternative topology would get us where we need to be before going down that road.

Like · Reply · 2y



Nigel Springett For high efficiency, optimise the trafo for low ac losses and good coupling, and use an extra inductor for the commutation.

Like · Reply · 2y



Charlie Elliott We Nigel Springett - you raise and interesting point. Will having an external inductor always give higher efficiency? Is there a difference as far as the secondary diode snubbing between the two cases?

Like · Reply · 2y



Nigel Springett using extra inductor allows the traof to be optimised for low losses, this usually means interleaved windings and low leakage inductance.

Like · Reply · 2y



Cameron Stewart Consider using a current doubler to reduce copper losses and snubbing losses.

Like · Reply · 2y



Colin Tuck A current doubler also doubles the voltage seen by the diodes - so at 400VDC out - perhaps not so good ...?

Like · Reply · 2y



Cameron Stewart No worse than a center tap configuration. Full wave bridge has the lowest voltage stress.

Like · Reply · 2y



Colin Tuck Indeed 400V a lot easier for diodes to deal with than 800V+ and lower RFI to heatsink too ...

Like · Reply · 2y · Edited



Charlie Elliott Current design is FB diode rectifier due to 400V DC out and the 50% swing on input volts dictating turns ratio.

Like · Reply · 2y



Write a reply...









Ray Ridley 1 It depends on how well the eternal inductor is built!

Like · Reply · 2y



Charlie Elliott Was "eternal" a deliberate slip or Freudian?

Like · Reply · 2y



Colin Tuck perhaps referring to one built by Michael Faraday...



Q

Like · Reply · 2y



Write a reply...











Yurii Shynkarenko Colin Tuck Colin, please, an interesting question still hangs in the air.

The 4W losses in an ETD44 mean that a TX temperature can raise up to 90C degree if the inverter has no the fan, isn't it? What TX temperature did you get without a fan at full load of your 1.5kW PSFB base on an ETD44?

The 4W TX losses are good, but still not enough for high reliability. In that case, the fan is the only hope for the reliable work, isn't it?

Like · Reply · 2y



Colin Tuck yes, it was a fan cooled unit as only 1 U high and 4 across a 19" rack (1U = 44.45mm, but unit height actually 42.45mm to allow for rack shelving etc) 4 units wide across a rack is a weird number - as three phase supply is difficult to balance this way - but customer is always right so ... sigh ...

Like · Reply · 2y · Edited



Colin Tuck @ Yurii, while 4W might seem high to you for an ETD44, if it is in an enclosure with holes in the right places giving convection airflow at full power - hot spot Tx temp can be lower than 90C in a 30C ambient.

Like · Reply · 2y



Yurii Shynkarenko Colin Tuck Colin, thank you for the reply. I know.. a customer is always right ...

Like · Reply · 2y



Cameron Stewart The customer is always right ... .....until it comes to custom power supplies ....

Like · Reply · 2y



Yurii Shynkarenko Colin Tuck Colin, Would you give us a link -- " useful technique invented Colonel MClyman". Thank you in advance.

Like · Reply · 2y



Colin Tuck you can easily google the name + tapped inductor.

Like · Reply · 2y



Yurii Shynkarenko Colin Tuck OK, Colin, Thank you.

Like · Reply · 2y



Yurii Shynkarenko Colin, thanks! Colonel MClyman is the genius! Useful technique invented Colonel MClyman here: http://citeseerx.ist.psu.edu/viewdoc/download...

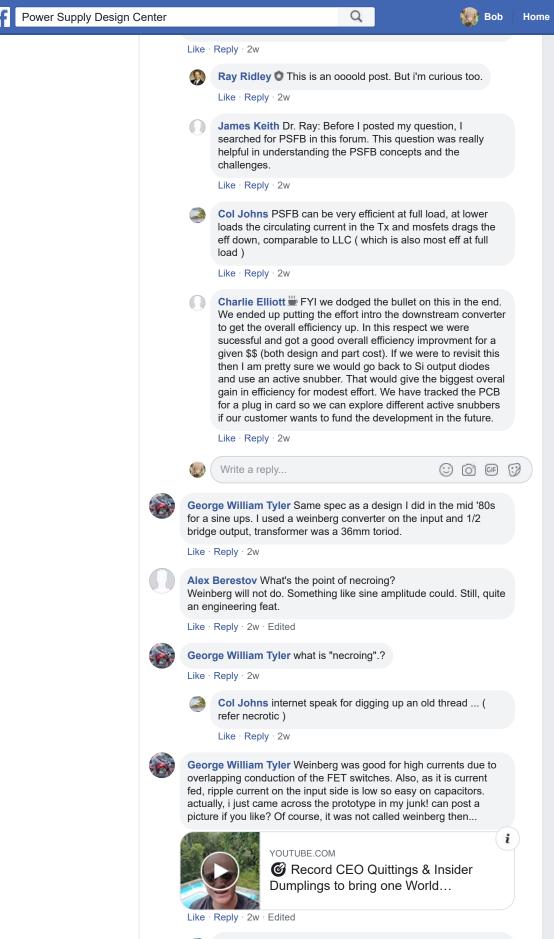
Conclusion:

The use of the tapped, output inductor and its benefits have been shown for both the push-pull converter and the single-ended, forward converter. There is very little to add to get exceptional circuit performance. The author incorporates the tapped inductor in all designs, when feasible. The performance of a converter, using the single or push-pull magnetic amplifiers, can also be improved with the tapped inductor.

Like · Reply · 2y · Edited



Colin Tuck you may need a snubber or two to limit overvolt spikes on the diodes, the main diodes now have a slightly higher reverse PIV, but certainly a useful ckt. Can be used in just about any choke input filter ...





**Col Johns** Overlapping Weinberg has been made to very high powers and very high efficiency - it has many advantages if the designing engineer can understand the operation well.

It is gaining new life in high power fuel cells where the input volts are low but currents are high.

Like · Reply · 2w · Edited

i





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Research on the optimal design of weinberg converter

Reply · 2w



## Cameron Stewart Col Johns

I have an overlapping boost Weinberg set up in Spice with zero current switching, a resonant snubber network, peak voltage snubbing, and recirculation of the clamped leakage energy to the output.

Theoretically, it allows the Weinberg to function in 440VAC three phase power factor correction and isolation applications, using 1200V silicon carbide devices, when all three phases are connected line to neutral.

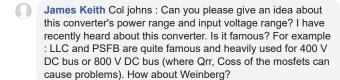
All I need it is to find a job to sell so I can build it. I've done a Weinberg three phase PFC three times before with passive snubbing and up to 92% efficiency in 220 VAC applucations.

The recirculating peak snubbing and zero current switching should improve that by 2% to 4% and also reduce the peak voltage stress on the push-pull mosfets.

It's the peak voltage stress and efficiency loss as a result, that is the Achilles heel of the Weinberg.

I don't know if this approach will help Charlie reach his goal of 97.5% with 120 VDC input voltage, but it might.

Like · Reply · 2w · Edited



Like · Reply · 2w



Cameron Stewart I've done 4KW with the three phase Weinberg, or 1300W per phase. Higher powers are theoretically possible.

It's the peak current and voltage stresses that set the maximum power limitation.

Like · Reply · 2w



Col Johns James Keith because its a push pull the mosfets see twice the Vin ( + spikes for a poor implementation ) so lower voltage apps are preferred - 1700V SiC allows 800V pk on Vin ..!

Like · Reply · 2w



Write a reply...





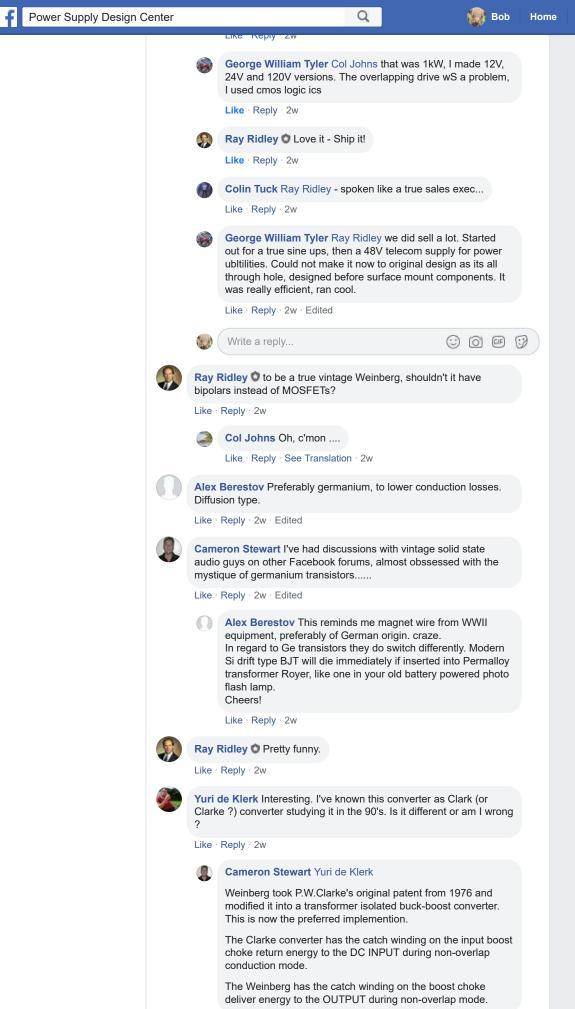


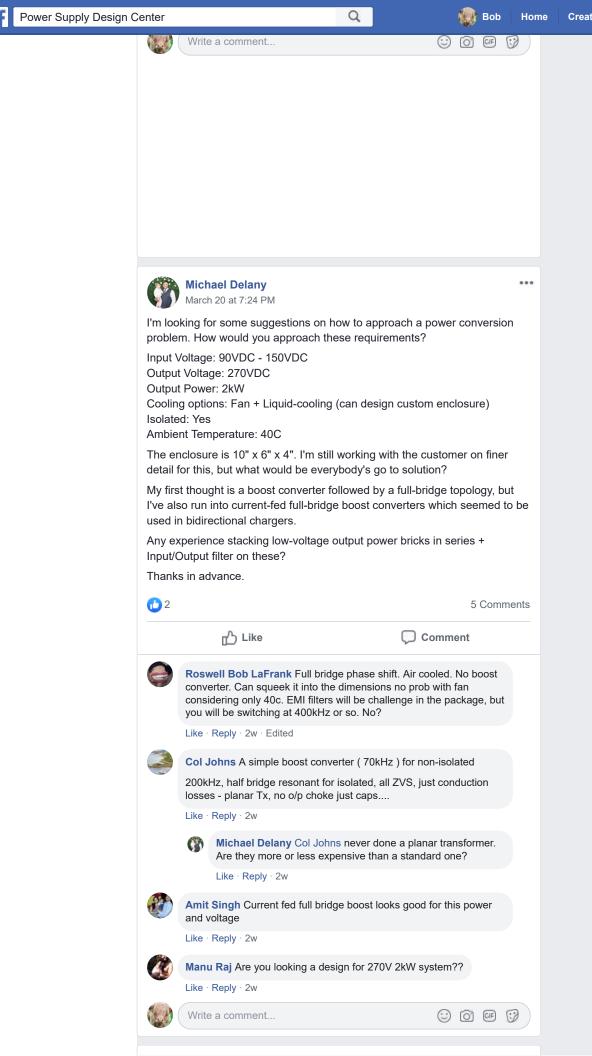


George William Tyler This is the prototype weinberg.



Love · Reply · 2w







John Baillie Arief Noor Rahman just make sure the transistor doesn't stay in the linear region long enough to heat up as the gste voltage increases... you don't need to the speed so the filter can be slow.





ruvar iz Debug the software startup step by step to see the glitch happens,

that way you will be able to know whether the problem is a form of software (bug in startup code) or hardware (worse to debug if it is a silicone problem)

Like · Reply · 2w



Write a reply...











Broox Le If you are 100% sure the glitch is from the I/o line, is it digital in nature - definitely driving a value you don't want, or analog in nature as in an unexpected spike?

If digital, be 100% sure your initial startup code technique is correct, 1st set desired internal pull-up/downs, set input/output registers, then enable output drivers. Coders often forget to set output register data to a known state before enabling the output driver. Also make sure your power on reset circuit function is intentional & well defined and your MCU power rail rise is monotonic. Make sure your power and ground integrity is solid and that you don't have surges on other I/o line(s) that might be producing a glitch on this one.

Like · Reply · 2w



Arief Noor Rahman mah, that's a very plausible culprit, i will check this and get back to you tomorrow after testing...

Like · Reply · 2w



Arief Noor Rahman @ Oh...the troubling GPIO pin glitch has digital nature

Like · Reply · 2w



John DeFiore I haven't looked at your specific flavor of the TMS320, but in general with this family some of the GPIOs on the part will default to having a pull-up enabled on power up, and some of them default to floating. So if you need it to be high on power up you can select the pull-up

Like · Reply · 2w



Michael Delany I posted a similar response without reading your answer first (but I think you're correct). These parts appear to have a very strong pullup unless I misread the datasheet. STM32 for example are around 50-60kohm, so putting a 10k works, but a 100kohm wouldn't. Double checked the datasheet and you're correct.

Like · Reply · 2w



John DeFiore version, and if you need it to be low you can select the floating GPIO and add a pull-down resistor. (Or use either but overpower the pull-up.)

Like · Reply · 2w



Michael Delany Are you positive the pull down is 10k? The default for this chip is a digital input with pull ups enabled. You might be creating a voltage divider depending on how strong the pull up is. You could try 1kohm and see how that works. Did you measure across the pull down resistor to see if it's creating a divider?

Like · Reply · 2w



Michael Delany It looks to me that your pullup is this 140uA which would equate to about 20kohm equivalent resistor. Maybe this is putting 1/3 of VDDIO on the gate of your FET. I still think changing the pulldown resistor to 1kohm is a good test.



















Broox Le Until you discover some kind of fundamental design limitation.

Like · Reply · 2w



Broox Le Crazy story: my first 'real' engineering project out of college was to debug a new industrial motherboard update where the primary change was that they updated the 'Wintel' chipset to the latest rev from the same vendor...and the problem was OS/2 would periodically hang at seemingly random times. I poured over that thing for weeks, had to buy books about PC-AT system architecture because they didn't teach that in college, couldn't find any signal or power integrity issues, kept asking the chipset vendor what things they modified from the previous version and they insisted 'nothing really changed, other customers are having no problems, this is in full production' [and the boss thought this would be an easy project for the new guy] No other test software or operating systems were having a problem. I finally got ahold of a really helpful guy at IBM who offered to do a remote kernel debugging session......after playing around with it for a while and getting it to hang a few times, he said, "huh, the timer tick interrupt has stopped - that's what triggers the preemptive task switching.' That gave me a direction and I found a flaw in the chipset's interrupt controller implementation such that if two particular interrupts occurred under another particular condition, the controller would latch off the real-time-clock interrupt and stop responding to it hardware bug in the chipset unfixable by software. EXCEPT, this was an STD bus CPU card of our own design (Pro-Log Corp) and they had a common practice of putting a Xilinx FPGA on board to do some other bus arbitration and external interrupt prioritization; we were able to use the on-board FPGA to implement a digital filter to prevent the particular timing condition that would lock up the chipset's interrupt controller. The FPGA code resided in an on-board serial EEPROM and was changed with a field system BIOS firmware update.

So, we worked around a bad fixed hardware flaw with programmable hardware that was there. 🙂

Like · Reply · 2w



Ray Ridley Of course the modern processors don't have any latent little bugs like this.....

Like · Reply · 2w



Arief Noor Rahman months not exactly, there are always silicon errata...and newer processor sometimes plagued with unknown bug...

so, older device could actually be better since all bugs are well known...

I have one helping a company for their ADC weird measurement, which turned out is caused by somehow the ADC cannot measure from 0~3.3V stated in datasheet, but limited to 0.5~3.3V

thus at that time, the quick fix is just shift the signal, and reduce the signal gain

Like · Reply · 2w



Write a reply...











Like · Reply · 2w

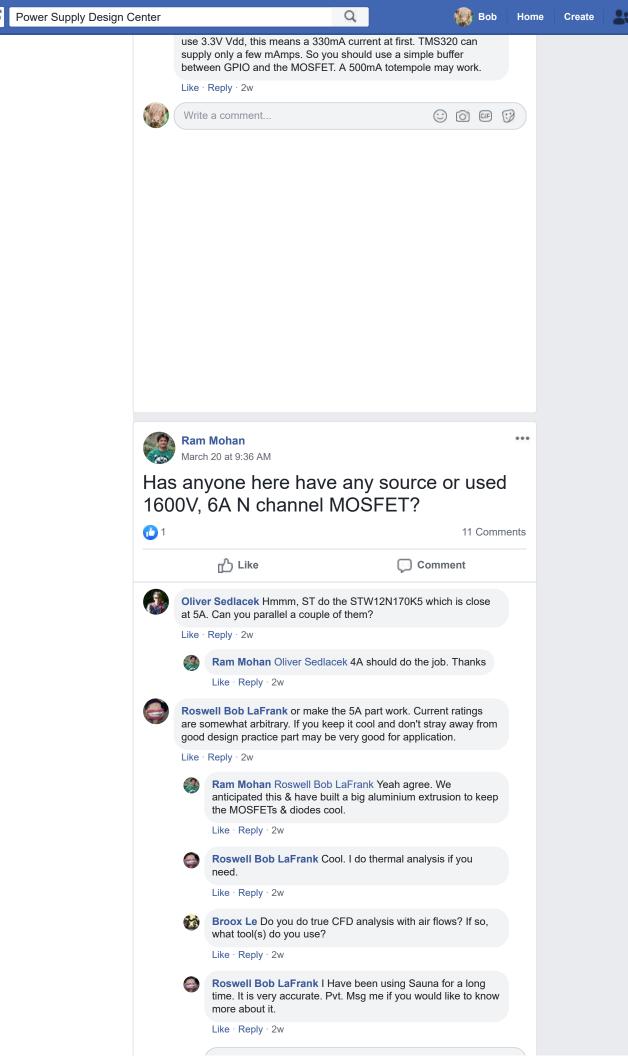


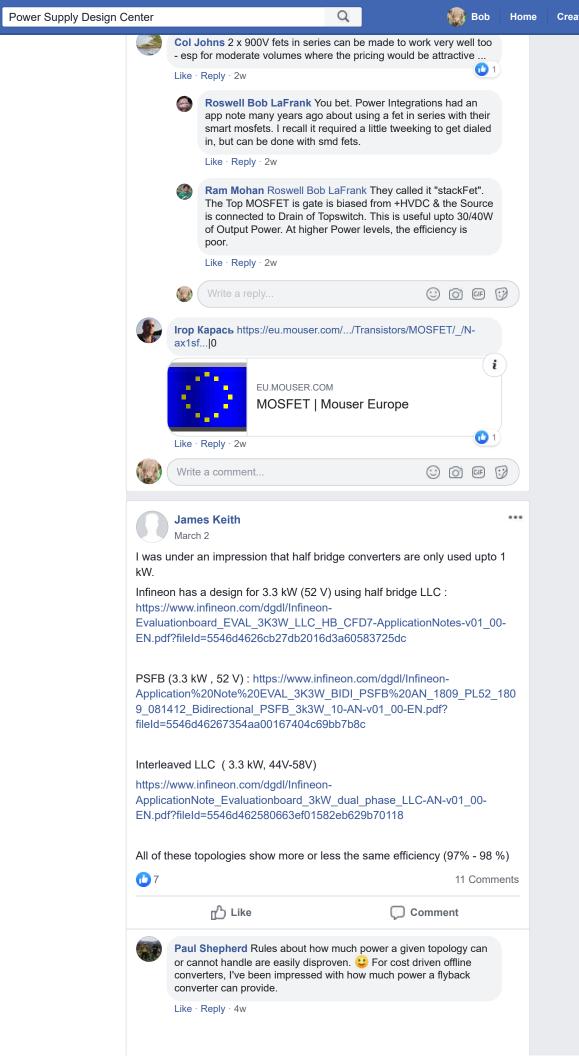
Ram Mohan Is that a MOSFET you are using to drive the Relay? Try replacing MOSFET with a simple transistor. Transistors will have lower Input Impedance than MOSFET & will snub the glitch. Also using a pwm pin makes no difference since you only need to turn off or on the Relay. I suggest you to put two Schottky diodes, one tied to vcc & io pin the other tied to gnd & io pin. Changing to Transistor should solve the issue

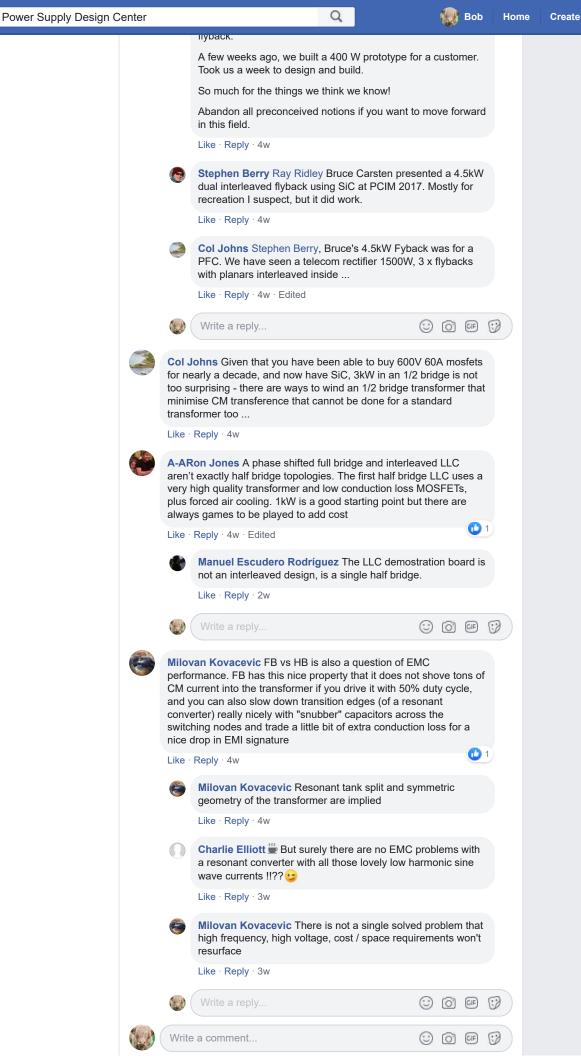
or do you optimize it based on the FET max Vds? Like · Reply · 2w ⊕ @ @ *®* Write a reply... Amit Singh Pull down resistor

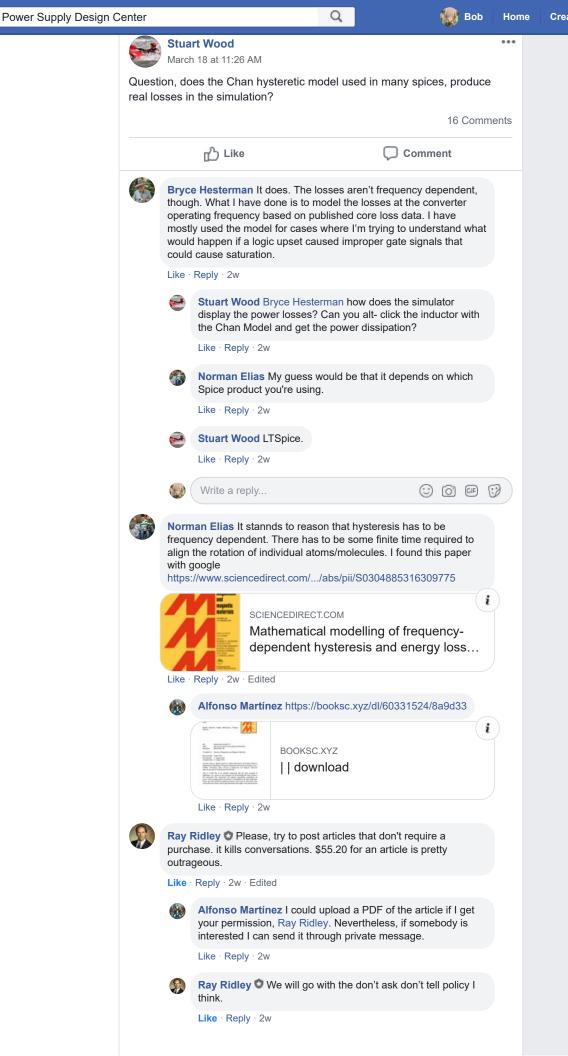


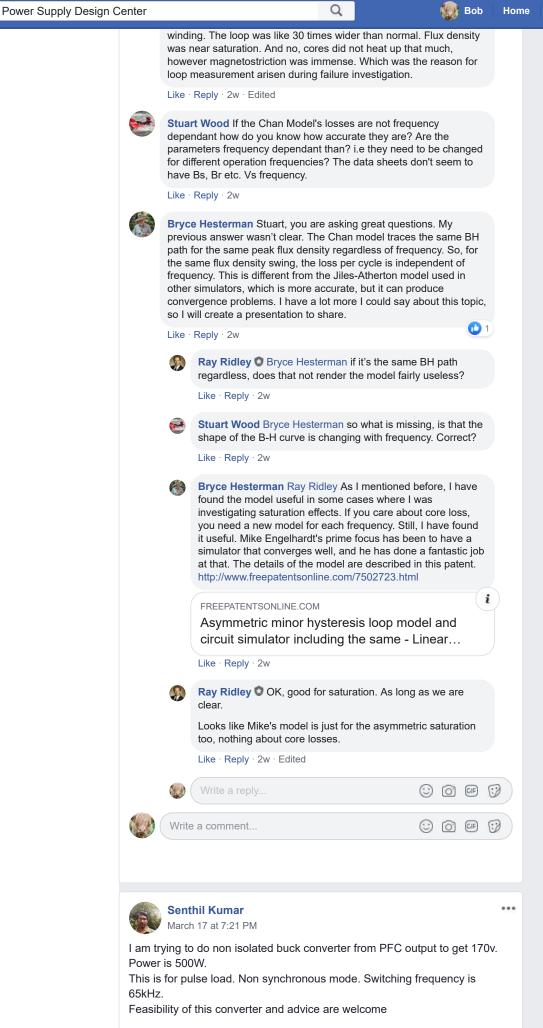




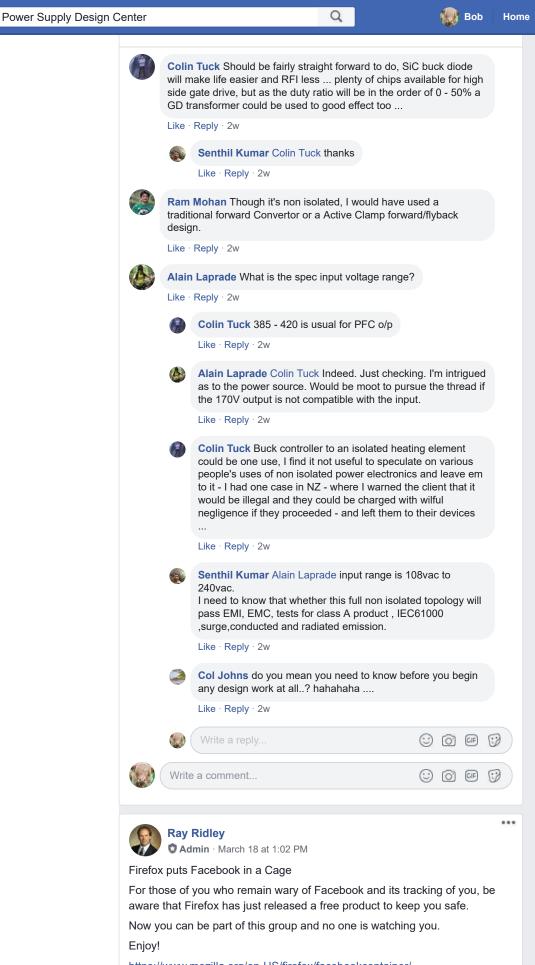








9 Comments



https://www.mozilla.org/en-US/firefox/facebookcontainer/



Q



## SUPPLY **DESIGN** CENTER



17 Comments







Norman Elias 😃





Jonathan Beaver I've been using that for a few months now and it's great.

Like · Reply · 2w



Sandeep Kr Neat!

Like · Reply · 2w



Alain Laprade Will give it a spin. Note that after installation, I got logged out of facebook automatically. Have your password handy.

Like · Reply · 2w · Edited



Peter Comrie Strange, I've had the Facebook container for months already.

Like · Reply · 2w



Andrew Ferencz Ray - I don't have Facebook on my phone (or any of those programs ... instagram, etc.) and I use FBP (look it up). When I went and saw my tracking - I am a ghost. I see no ads. I am zero tracked ...

I wonder if I crossed the Chinese boarder and took my phone would they believe me?

Like · Reply · 2w



Tony Salsich I have been using for a few months as well. Love it.

Like · Reply · 2w



Alex Berestov So the Firefox will be selling your data to Facebook or to BigBrother directly.

Like · Reply · 2w



Edward Ralph Alex Berestov that's not how Firefox works.

Like · Reply · 2w

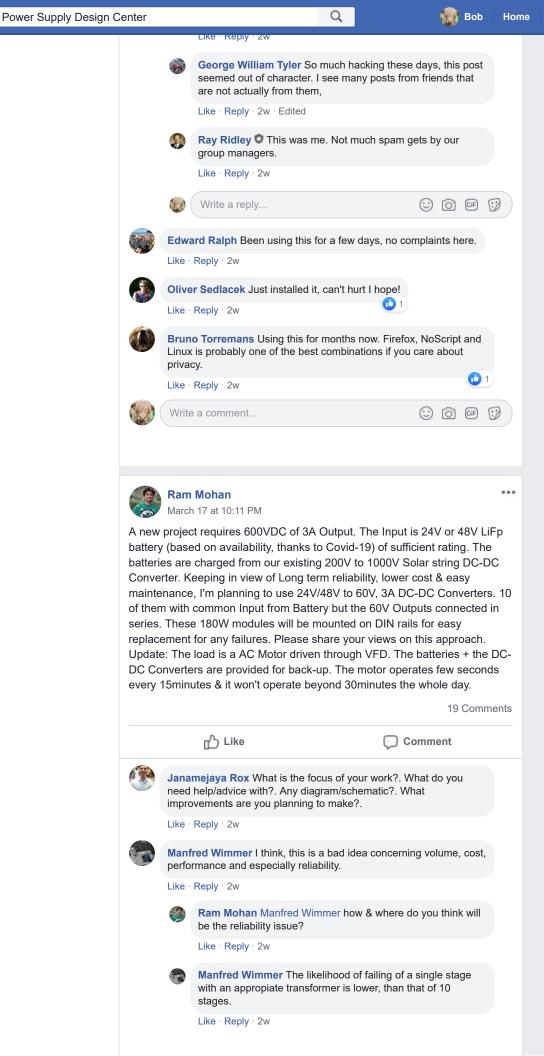


Alex Berestov It's a joke, period P.S. Free stuff is a mousetrap. P.P.S. Ask another Edward.

Like · Reply · 2w



George William Tyler I don't believe Ray sent this.





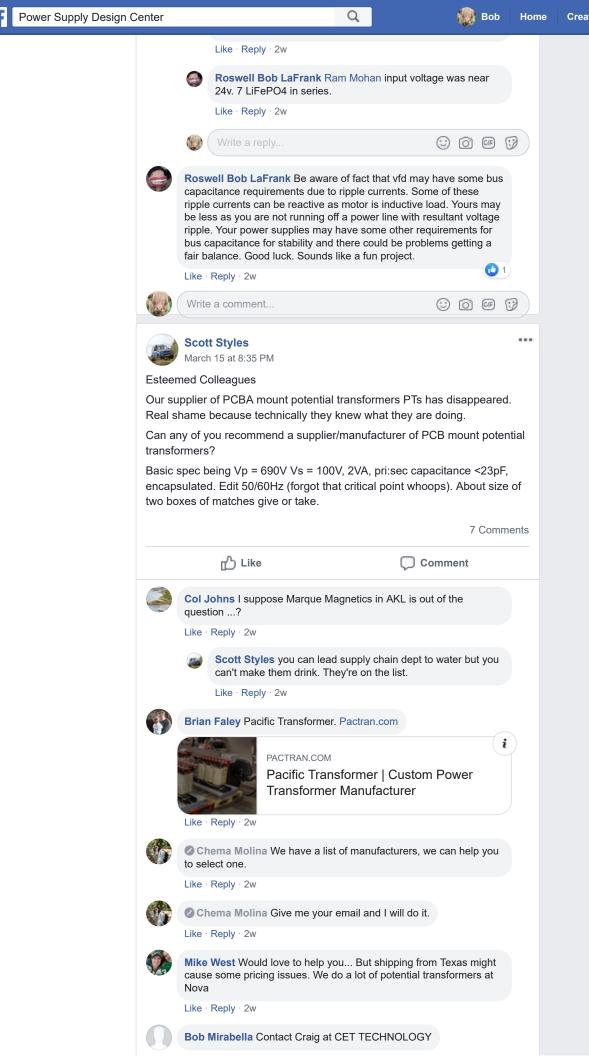


Roswell Bob LaFrank Why wouldn't you do it with one converter? 600v out at 3 amp is a fairly easy design. I did a very similar design with a resonant push-pull.

Like · Reply · 2w



Colin Tuck pretty sure he wants off the shelf ....







Alberto Difrancesco March 6 at 3:51 PM

Hi all.

I'm in fight with a well known problem: ground routing. In my current design, I'm developing a 30W offline SMPS.

My question is: how to tie power gnd with signal gnd? The signal gnd comprises the controller, driver and Vaux ones. In previous designs, I kept pwr/sgn grounds separate and tied them underneath the main bypass input capacitor (as a stable ground point) BUT some components seemed to suffer from ground bounce effects (especially the half-bridge driver).

So, I want to change my approach now: some AN recommend to derive the sgn gnd directly from the low-side source and then tie pwr/sgn grounds undertneath the thermal pad of the controller (if present).

What do you think about that? What do you think is the best approach to tie differents gnds guaranteeing stability and avoiding loops?



Bob Gudgel

10 Comments







David Edwards # How many layers on your board?

With two layers you can treat one as the ground plane and route everything on top only going to the back side to make very short jumpers. Slots in the ground plane act as antennas and interrupt mirror currents from topside traces.

Another approach is to freely route traces on both top and bottom and fill in all areas not used for traces with ground pours. Some layout software will automatically connect overlapping ground islands together with a single via, but you really need many multiple vias spaced every centimeter or two. Filling in all empty spaces with copper keeps the board from warping during soldering.

Like · Reply · 4w



Alberto Difrancesco Hi David, the current board is 2 layer. I agree with your first solution but the necessary condition is to have a very stable ground plane. So, in this case, the main effort is to well isolate the power ground defining all the current return paths, and connect it to the main gnd plane in a stable point (underneath the input caps?). Then, I think I will be able to use short jumper for gnd connection.

Like · Reply · 3w



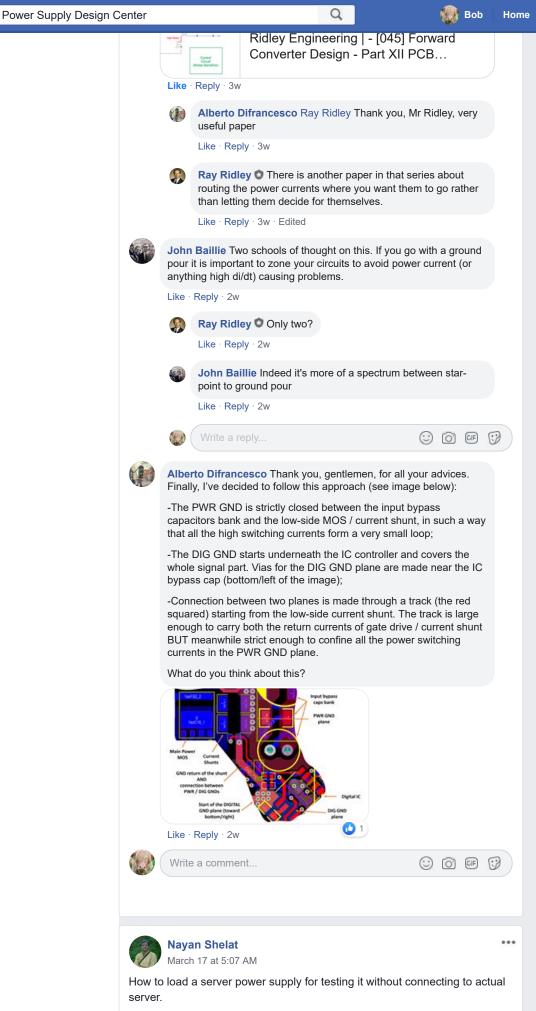
Darrell Hambley What IC are you using? I had a similar issue with an LT8646. It has a common ground connection to its bottom heatsink pad. All the high-current traces and grounds and thermal vias were laid out around the lower potion of the IC (pins 4-23). The control signals and components were routed around the upper (pins 24-3) portion of the IC. A ground plane on layer 2 was under all control traces and components but, this ground was an isolated island with only one connection to one IC pin. This allowed the control signals to be over a clean ground.

Like · Reply · 4w



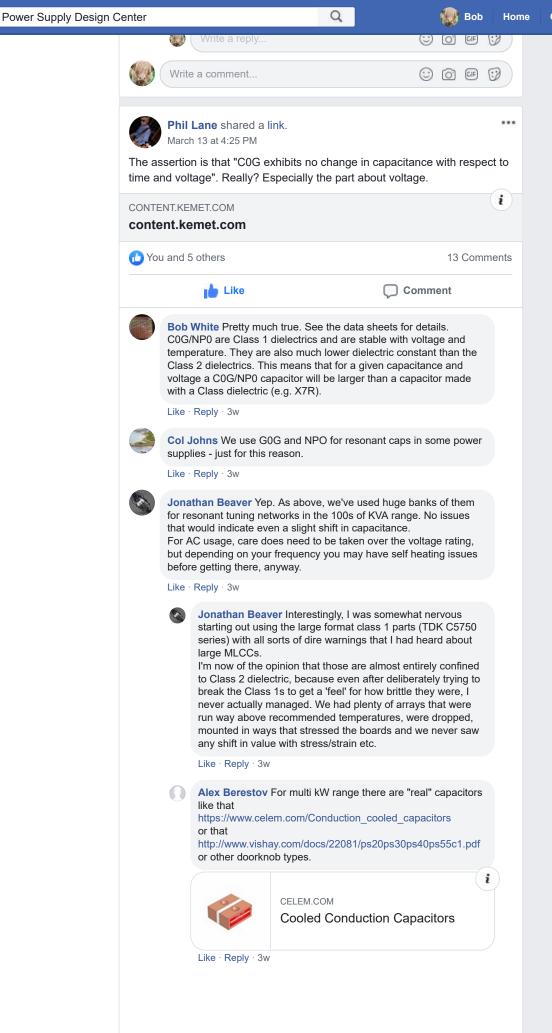
Ray Ridley check our grounding issues paper in our design center. That might help you. One of the secrets is to not let the power currents pass through the control ground. A consequence of that is avoiding a full pour of ground on the board, counter to the way most layout engineers would go.

http://ridleyengineering.com/.../79-045-forward-converter...



We are attempting to characterize a newly developed server power supply for conducted emission.

Yuri de Klerk Col Johns I couldn't have guessed it's really about the connectors, haha.





still sitting in boxes downstairs.

They're extremely expensive per KVA (edit: at least at our fixed frequency of 85kHz), much lower Q than the ceramics and extremely awkward when you need to be able to adjust values.

Like · Reply · 3w · Edited



Alex Berestov Those are pretty much standard in induction heating. Used to witness bank destruction, made of hundreds of caps: one cap dies, current is up for the rest. Sounds like machine gun.

In regard to price: 0.33 uF 1kV NP0 is around \$100 and is rated around 20A RMS. Not to mention current sharing and so

And yes I've seen 2...3 thousand PP film caps where 2 or 3 big ones could suffice.

Like · Reply · 3w · Edited



Jonathan Beaver Alex Berestov Well my area isn't induction heating, it's wireless power. In induction heating, there are generally simpler resonant networks and less importance to being tuned onto a specific frequency. For wireless power we typically end up using multiple banks, often split, and it's generally easier to adjust the fitment of a bank of smaller units to bring it to the primary frequency than it is to adjust the magnetics, which are VERY carefully optimised. For those units, I suspect you're thinking of something like the Porcelain ATC caps, not regular NP0s. Those aren't particularly useful for us, either, and are targeted at much higher frequencies (RF region).

The TDK units we're dealing with are 630Vdc or 1000Vdc rated (used at 220Vrms or 350Vrms respectively) and are normally in the 10-100nF range for less than 1USD each. Overall cost is 10% of the Celem solution for the same total production kVAR quantities, including board and assembly

Current sharing is something to be aware of when designing the array, but that's where the art is. I've never had too many issues with it in most circumstances, even up to banks that are in the 10 series/20 parallel kind of component ranges. Biggest array was something like 300 KVA just for the parallel resonant part of the array, never mind the partial series compensation or other parts of the tuning network.

Like · Reply · 3w · Edited



Write a reply...









Nathan Ellis Thanks for the input; I had been wondering the same.

Like · Reply · 3w



Alex Berestov Yet another way to "... fuel efficiency". While most designers squeeze fraction of a % in efficiency, there come people wasting hundred times of that just for "convenience" polluting surroundings on the way. "

Like · Reply · 3w



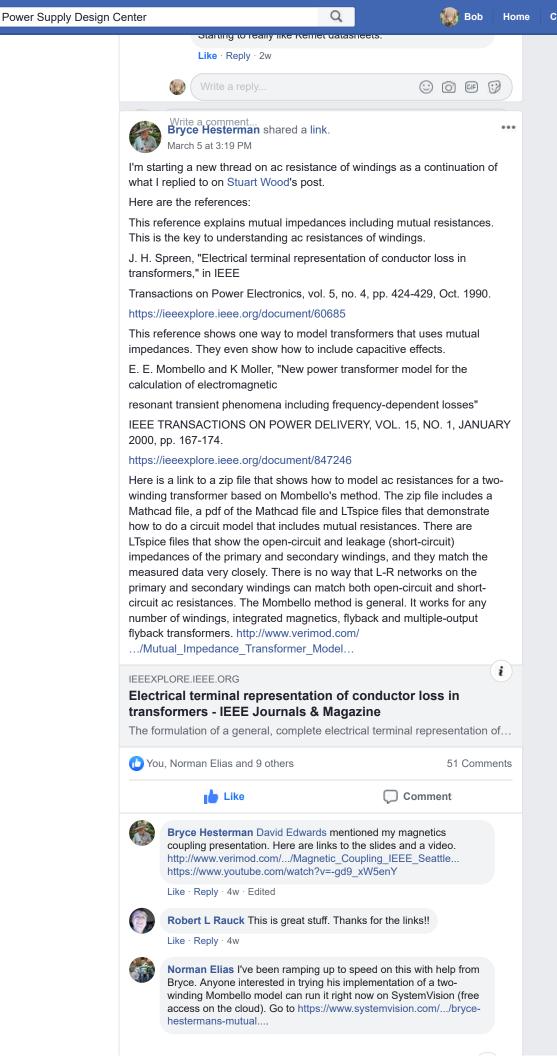
Phil Lane The massive Murata datasheet has a link to "specifications and test method" on Page 108, for GRM series caps (presumably COG) - that doesn't work. Using more expensive Kemet, because the Murata datasheet is so poor. https://www.murata.com/.../capacitor/mlcc/c02e.ashx...

Like · Reply · 3w



Alex Berestov The need of fine tuning is well understood, however inductors are easier 'cause you basically make magnetics "yourself". Here are caps that may work on par with power film ones, which are BTW self healing. They are capable of 10+A rms through the cap. @ \$5 1000pcs they are nor cheaper but what do I know. https://content.kemet.com/datas.../KEM C1039 KC-LINK C0G.pdf

Like · Reply · 2w · Edited





## Bryce Hesterman's Mutual Impedance Transformer Model | SystemVision®...

Q

Like · Reply · 4w



Norman Elias RidleyWorks uses L-R networks on the windings to approximate Dowell's mathematical solution to the frequency dependences. Mombello introduced an equivalent circuit suggested by the electromag physics. You can fit the model parameters to measurements or to a mathematical formulation such as Dowell's. Has anyone tried simply writing Dowell's formula (or any good alternative) into a transformer model, e.g., in Verilog-AMS or VHDL-AMS?

Like · Reply · 4w



Ray Ridley Duts of ways to do all this. What is unique to ours:

It takes about 2 minutes to define the winding structure. Then three mouse clicks to load the entire model into LTspice ready to run.

The other methods here will teach you much theory, but take many hours to implement practically.

We are all about speed of development, and time to market. We incorporate advance analysis along the way with zero pain to the user.

If you want to dig into and understand Dowell's, go for it. If you just want a fast and accurate model to simulate the proximity loss, you can do that instead.

Its kind of like using a FET in your power supply. You can apply a gate drive signal and turn it on and off at will. Or you can go dig into Schroedinger's wave equation applied to semiconductor physics first for a few weeks, then come back and turn it on and off the same way. It's all good. 😃

Like · Reply · 4w



Norman Elias Good point Ray. I, for one, prefer collaboration to confrontation. Your goal is not, and should not be, to provide the most accurate model possible. Bryce seems to have some good ideas. If we put our thoughts together, who knows, maybe we can produce a model that will fit your objectives for RidleyWorks. It's not a matter of who's right or who's wrong. It's a matter of what can we accomplish using our best ideas. This forum is a great place to explore those

RidleyWorks is a great tool. I'd love to find a way to contribute to it. Bryce is promoting some new ideas. I'd love to see where that takes us.

Like · Reply · 4w



Ray Ridley Norman Elias all we ask of people's models is they come in excel

Mathematical function in there are extensive.

In the end a good tool is judged by how well it presents data and that is where excel excels.

Like · Reply · 4w



Bryce Hesterman My hope is that someday what I am working on can be put into a form suitable to include in RidleyWorks. The Dowell-based approaches with LR networks can have great utility in the limited cases where Dowell's assumptions hold. For more general cases, such as any transformer driving multiple loads or transformers with large magnetizing currents, or parallel-connected windings, a more rigorous approach is required, but any approach that is general requires understanding some subtleties of linear circuit theory including mutual resistance to accurately model the proximity effects. In Mathcad, I have worked out how to write .inc files for implementing the Mombello model in spice. Porting the model exctraction to Excel is difficult, but Norm Elias is helping me. The bottom line is that understanding the limitations of any modeling approach is important.

Q

however, it would be helpful if you could explain what it is and what the coupling mechanism is. I am guessing it is just proximity effect induced currents in nearby conductors.

Like · Reply · 4w · Edited



Bryce Hesterman . In general, for any linear multi-port network there are self-impedances and mutual impedances between each pair of ports. This applies to any circuit, including transformers. It is as fundamental as KCL and KVL. In general, mutual impedances can have any complex value. When magnetic coupling is to be modeled, we all know about mutual inductance. When interwinding capacitances are being modeled self and mutual capacitances are considered. For whatever reason, people have largely forgotten about mutual resistance, but it is an essential concept for understanding the proximity effect. Here is the basic idea in equation form.

In the frequency domain, the terminal voltages,  $v_1$  and  $v_2$ , and terminal currents,  $i_1$  and  $i_2$ , for a two winding transformer with winding losses are related by the expressions

$$v_1 = (j\omega L_1 + R_1)i_1 + (j\omega M + R_{12})i_2$$
 (1)

$$v_2 = (j\omega M + R_{12})i_1 + (j\omega L_2 + R_2)i_2.$$
 (2)

Here,  $\omega$  is the radian frequency;  $L_1$ ,  $L_2$ , and M are the usual self and mutual inductances of electrically isolated but magnetically coupled windings;  $R_1$ ,  $R_2$  are the usual vinding resistances; and  $R_{12}$  is a mutual resistance, usu-

Like · Reply · 4w



https://ecee.colorado.edu/~rwe/references/PESC98.pdf.

If you need an extension in python/matlab I can support you no problem.

Up to now I have wrote some script to fit simple spice model from measurements, I'm planning to improve it also  $\ensuremath{\mathfrak{C}}$  https://www.linkedin.com/.../spice-model-extraction.../

Like · Reply · 4w · Edited



**Don Marabell** Riccardo Tinivella Bryce also did a nice presentation at denverpels.org(2007)



DENVERPELS.ORG

IEEE Power Electronics Society - Denver Chapter Home Page

i

i

Like · Reply · 4w



**Bob Gudgel** It doesn't look like the Denver chapter has had any meetings for several years now? No interest?

Like · Reply · 2w



**Stuart Wood** For impedance curve fitting, I found a python program called Zfit\_v2.0 it's easy to add new circuits to it and was able to fit a 3000 point data set to a 5 order LR network in about 20 seconds.

Like · Reply · 4w



Riccardo Tinivella Thanks for the tip! is this link? https://exality.com/fitting-equivalent-circuits-to.../



EXALITY.COM

Fitting Equivalent Circuits to Impedance Data | Exality...

Like · Reply · 4w



**Stuart Wood** Riccardo Tinivella yes, it's easy to modify, and in the public domain.

Like · Reply · 4w · Edited

Like · Reply · 4w



Ray Ridley 20 seconds to match? Did you mean to say 20 ms?

Q

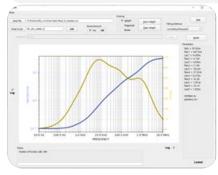
Like · Reply · 4w

Nicola Rosano Ray Ridley it's struggling.

Like · Reply · 4w



Stuart Wood Ray Ridley No I meant 20 seconds, worst case.I have no problem with it taking 20 second as long as it comes up with a good match. This took less than 2 seconds



Like · Reply · 4w



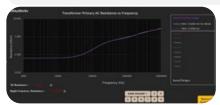
Ray Ridley Dook, there are closed form solutions to the problem that are instantaneous. We have ours in our software, Nicola Rosano has his.

However, I understand, people like to engineer their own solutions. That curve you are showing is not a good match. The algorithm, as Nicola Rosano has said, is struggling.

Like · Reply · 4w



Ray Ridley This is the kind of match you should be seeing.



Like · Reply · 4w



Ray Ridley Nicola Rosano has gone one better with a 7th order network to reduce the error from around 7 % or so to 1

He is a quintessential engineer.



Being in the lab all the time, I'm happy with 10%, but I am impressed. We just didn't want to hit LTspice with 21 new state variables instead of 15. That seemed an unkind thing to do.

Like · Reply · 4w



Riccardo Tinivella Nicola Rosano sorry to haven't read all comments or post of the group, nut I haven't seen the free tool you posted. Can you reshare it?

Like · Reply · 4w · Edited

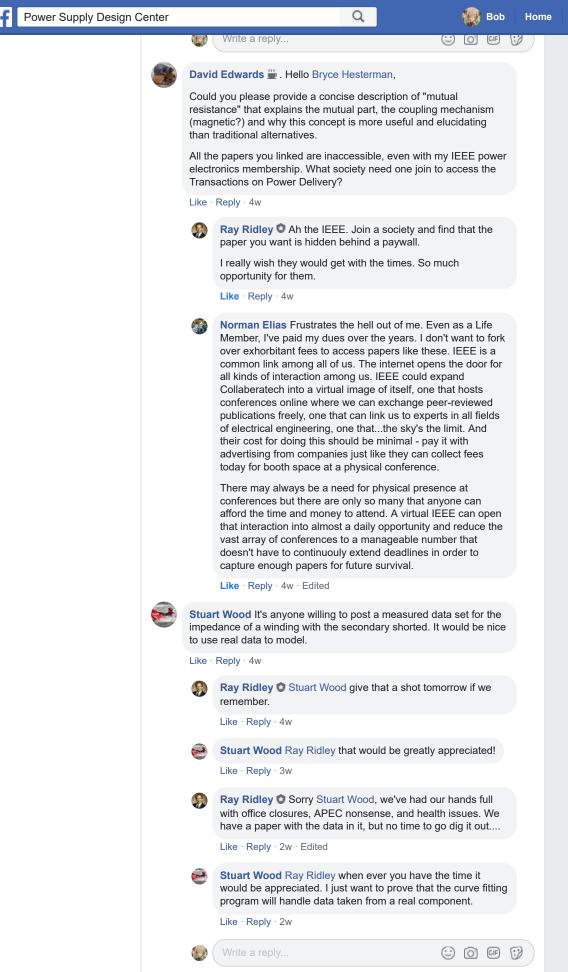


Nicola Rosano Ray Ridley thanks Ray appreciated

Like · Reply · 4w



Stuart Wood Ray Ridley the curve on yellow and blue is the data taken from one of the LR networks you posted in a paper. The thin black lines are the solution that ZFit found to match the blue and yellow lines.



with primary shorted. Look at the PDF in the zip file. http://www.verimod.com/.../Mutual\_Impedance\_Transformer... Keep in mind that no RL network can model both open-circuit and short circuit impedances unless a coupled network is set up to model the mutual resistances.

Like · Reply · 4w

**(1)** 2

#### Hide 16 Replies



Ray Ridley Bryce Hesterman not sure what you are trying to say here. Is this a suggestion that the models we are using are not useful?

Pretty bold claim about Dowell and his work if so.

Like · Reply · 4w



### David Edwards . Hello Ray Ridley and Bryce Hesterman,

I think Bryce is intimating that you cannot model all transformer loss with a single network. This, of course, is neither a problem nor an issue nor against your expectations, which presumably are that one must create one LR network for winding loss (in series with current) and another RL network for core loss (in parallel with voltage).

I think that (non-physical) mutual resistance may be a useful concept when one is modeling a transformer with linear algebra. However, when visualizing (and modeling) what is actually going on physically regarding transformer loss, mutual resistance is a misleading concept in my opinion (but perhaps I don't fully understand it).

Take all of the above with a grain of salt.

Like · Reply · 4w · Edited



Bryce Hesterman Ray Ridley What I have been trying to say is that Dowell's work applies to a special case in magnetics, and magnetics that don't fall within the parameters of that special case can't accurately be modeled with Dowell's method. His paper is very clear about what is required to be in this special case. (1) The magnetizing inductance is so high that magnetizing currents are negligible. This rules out magnetics with gapped cores or low permeability cores. (2) The H-field is parallel to the winding layers. This rules out magnetics with windings that produce distorted fields. For example, a one layer primary with full-width and a one-layer secondary with half of the layer full. If the secondary of that example keeps the same number of turn, but is spiral wound to fill the full width of the primary, then Dowell's method is reasonable. (3) The MMF has to have defined patterns of where the MMF is essentially zero. This rules out transformers with parallel-connected windings, and transformers with independent loads on seperate windings. What you need to make Dowell's method work with multiple windings is (a) that all primary windings are connected in series, and all secondary windings are connected in series, with no currents flowing out of the junctions of the seriesconnected windings, or (b) the loads on two series-connected windings with a current flowing out of the junction are identical in magnitude such as a center-tapped rectifier, but you have to think carefully how to apply Dowell's method in that case. It all boils down to understanding the MMF diagram. Now, suppose you apply Dowell's method in cases that doesn't comply with Dowell's assumptions. The result will most likely be the losses will be under-predicted, but that is far better that having not tried to predict proximity losses at all.

real as Ohm's law. I plan to write up something to better explain mutual resistance, but this will take some time. Here are some examples that may help in the meantime. Suppose you have a primary winding and a secondary winding and a high reluctance core. If you measure the ac resistance of each winding, they will both be fairly high. If you short the secondary and measure the primary resistance, the ac resistance is way down because the secondary current creates a field that decreases the H-field in the primary. Dowell's method works well for predicting the effective resistances of both windings. Now suppose you have a primary winding and two secondary windings with independent loads. The effective ac resisitances of each of the windings will depend on the current distribution between the two secondaries because the field cancellation depends on all three currents. Dowell's method doesn't apply here because the proximity effect depends on the ratio of the secondary currents. Mutual resistance is the mathematical way to account for the losses in this case. You can implement SPICE models that are set up to model mutual resistance, such as the ones in my link.

http://www.verimod.com/.../Mutual Impedance Transformer... One of the benefits of using this type of model is that the leakage inductance effects on diode turn-off ringing are greatly reduced compared to two windings with a coupling coefficient, and are much closer to reality. Thus, by adding a few components, you can actually greatly speed up simulations. Another benefit is that you can model windings that are connected in parallel and see how the currents are distributed and what the ac losses are. I think my next step will be to create a Mathcad file and SPICE models for a threewinding case. The SPICE models will show how the ac resistances of the three windings changing with the ratio of the secondary currents, just as occurs in a real transformer.

Like · Reply · 4w



Like · Reply · 4w

Bryce Hesterman Ray Ridley Please read my final comment of my last reply to you. The bottom line is that if you missapply Dowell's method, you will be far better off that not having used it at all, even if the results aren't quite right.

Like · Reply · 4w

Ray Ridley That is why we don't misapply it.

Same could be said of Ohm's Law - if you misapply it, better off that you don't use it?

Like · Reply · 4w

Ray Ridley 1 don't really see how using Dowell's can get you in trouble. Worst case if overestimates the loss?

Once I had hardware in hand, I would take various impedance analyzer measurements and tweak the model to match, taking symmetries and asymmetries of winding structure into account (for allocating leakage and interwinding capacitance).

As a thought experiment, imagine a simple 1:1 two winding transformer with a shield between the windings. The shield will have no transformed current, but will have proximity currents at higher frequencies. This case may require adjustment of your models.

PS to Bryce Hesterman: the Facebook user interface is annoying, but you can start new lines with ctrl-enter. Just touching enter immediately posts your message. If you are not done, then to edit the message, you must click the ellipsis (three dots) that appear when you hover the mouse pointer over the center of the right edge of your message.

Like · Reply · 4w · Edited



Ray Ridley If you are not sure about these little things, Google as always is your friend.

Like · Reply · 4w



Ray Ridley We are trying to move the world away from do resistance to starting to use the results of Dowell's. It is a big step.

One of the barriers to this is that researchers are always talking about how they have something better than Dowell's. Regular engineers see that and they are confused. So they stick with dc resistance.

Get with the program here and help the process of moving the industry forwards.

DC Resistance - Good, better than using zero.

AC Resistance from Dowell's - Much better, can show 10x loss (for example)

Other esoteric methods - better again (maybe) you can see there is still argument about all that. It's what academics do.

Like · Reply · 4w · Edited



Norman Elias David EdwardsYou may also use alt-enter.

That's what I just used to skip to a new line.

I typed ctl-enter to skip the above lines. Some GUI's will skip lines if you type shft-enter,

I just used that successfully here. I don't recall having so much success with these prior to tonight. Maybe FB has improved it's GUI.

Like · Reply · 4w



Norman Elias Ray Ridley I agree with your message. The engineers need to use the tools they have with confidence and with discretion. As you've said consistently, engineers need to limit their reliance on simulation and conentrate on their laboratory prototypes.

Let those of us who work on the design aids spend time arguing over the best methods. When we are in agreement we can install our best choices in our tools. That's how BJT models advanced from Ebers-Moll to Gummel-Poon and that's how we can move on from Dowell to the next improvement and the next one after that.

I'm sure you'll swap-out the Dowell's model when you're convinced that there's something better that your customers should use. Nobody with any sense would keep replacing the model every time someone claimed to have something better.

Imagine a transformer with windings all with the same wire size, with one primary (two layers) and two secondaries (one layer each) one wound on top of the other. Now consider current distribution at a frequency such that the skin depth is a fraction of the wire diameter. This condition falls on the far right of Dowell's curves, but it is still important for realistic damping of ringing.

The MMF curve in the z-axis across the winding build is easy to draw and it is easy to calculate the reflected proximity currents in each winding by inspection. The proximity currents in each winding depend in part on the currents in the other windings. Proximity effects are not symmetrical between the two secondaries. This can be seen by examining the currents when only each secondary in turn is conducting current (as you have previously noted). To easily see this would probably require a simple diagram of MMF and current across the winding for the two cases.

After some more introspection I may draw up an LTspice schematic that is physically based to illustrate this situation. Of course, none of this is new information to you, but I wanted to let you know that I have at least partially absorbed the idea you are touting.

I still take issue with the term mutual resistance as being highly misleading (bad marketing for selling your idea) as it evokes coupling parallels to mutual inductance (which will close many minds before they have given the idea a chance). Perhaps a better term would be "shared resistance." Maybe someone will suggest something even better.

Like · Reply · 4w



Bryce Hesterman David Edwards I'm glad that it is starting to make sense for you. Slogging your way through Spreen's paper should make the three winding transformer examples more clear. There is a historical body of literature going back to the 1940s that uses mutual resistance, which is just a subset of mutual impedance. I don't think it would be helpful to create new terminology. My goal is to help motivate people to think of transformers in terms of linear algebra because it opens the way to gaining considerable insight that is available in no other way. Thinking in terms of fields provides another kind of insight. Thanks for the Facebook tips. I don't know how to do the same things on my phone.

Like · Reply · 3w



Norman Elias If you just think back to the mesh analysis problems you solved in your undergrad circuit analysis course you'll see that there's generally nothing magical about mutual resistance. It's just a resistance that appears simultaneously in adjacent loops. In the equivalent circuit for a two winding transformer the mutual impedance will have a real part even if you just model core loss.

Additional losses such as skin effect or proximity can only be modeled by adding more resistance to the circuit model. The closer your model topology comes to the physics of the device the more accuracy you'll get from your simulations. Proximity effects mean adding mutual impedance between adjacent turns of the windings. The Mombello paper introduces a model that comes down to increasing the real part of the mutual impedance between the main primary and secondary of the lumped element model. It's one step better than an R-L ladder added to individual windings.

Like · Reply · 3w · Edited







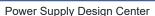




Write a comment...









Power Supply Design - New RidleyWorks Manual

You can now download our latest RidleyWorks software manual for free. Take a look at this - you won't find anything that even comes close in terms of designing, modeling, analyzing and simulating your power supply for you. You can simulate instantly any power level, and it selects all the power components for you, including the magnetics.

Unlike IC vendor software, you don't have to choose a part before you can do any design.

Trade off topologies and control choices faster and in more depth than you ever though possible.

http://software.ridleyengineering.com/.../RidleyWorksManual.p...





26 Comments







Scott Styles .. ANY power level.... Really?

Like · Reply · 1y



Ray Ridley Thanks for noticing that Scott Styles - name your power level!

Like · Reply · 1y



**Graham Ward** Go on Scott, tell him what power levels you're more accustomed to engineering...

Like · Reply · 1y



Scott Styles not a boast or brag Graham, but Ray I guess it does go to raise another question which is 'what size stuff are people on here working on/with? (our stuff is typically a few MVA made of few hundred kVA chunks)

Like · Reply · 1y



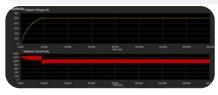
Ray Ridley That's great Scott Styles, nice to have you aboard!

Like · Reply · 1y

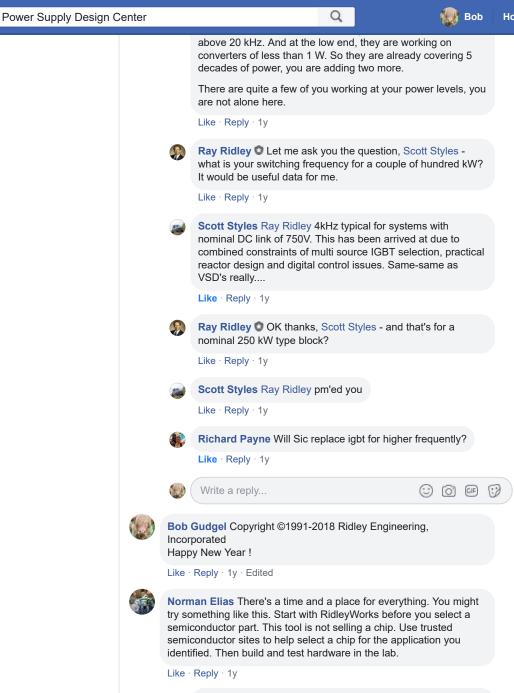


Ray Ridley Power is power - we all face the same issues it just comes in different sizes, and at different frequencies. Now some of more of you big boys are here, we can have some meaningful discussions about the different ways of doing things, and the challenges we all face.

Can we simulate your systems? Sure, here is a 500 kW buck converter simulation, switching at 5 kHz.



Like · Reply · 1y

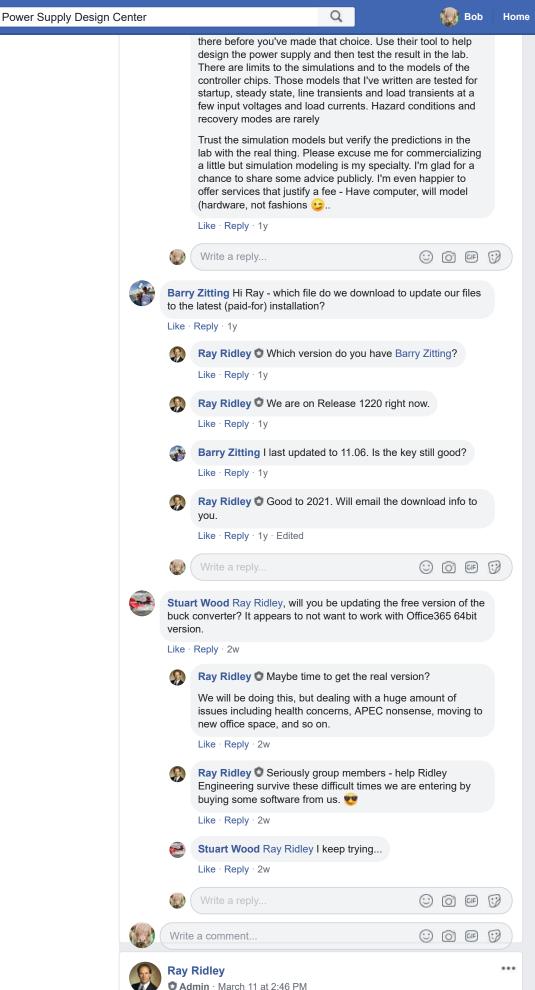




Like · Reply · 1y

Ray Ridley Dut hey, the software is free - what do you expect at that price?

Like · Reply · 1y















👍 😭 You, Phil Lane and 55 others

17 Comments





Comment



John Beecroft We are many! Just gotta remember to wear a shirt when on a teleconference.

Wow · Reply · 3w



Ray Ridley And don't stand up.

Haha · Reply · 3w



Scott Styles google 'the oatmeal working from home'



Like · Reply · 3w



David Sands No mention of this little beast that I saw in the latest Ridley Newsletter? Seems like this with a power supply would be all a home lab needs...

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Like · Reply · 3w



Ray Ridley mmmm..... I wonder what that box on our character's desk might be.....?

Like · Reply · 3w



Norman Elias Maybe a router.

Like · Reply · 3w



David Sands Ray Ridley Expensive beer coaster?



Like · Reply · 3w



Ray Ridley David Sands it does EVERYTHING.

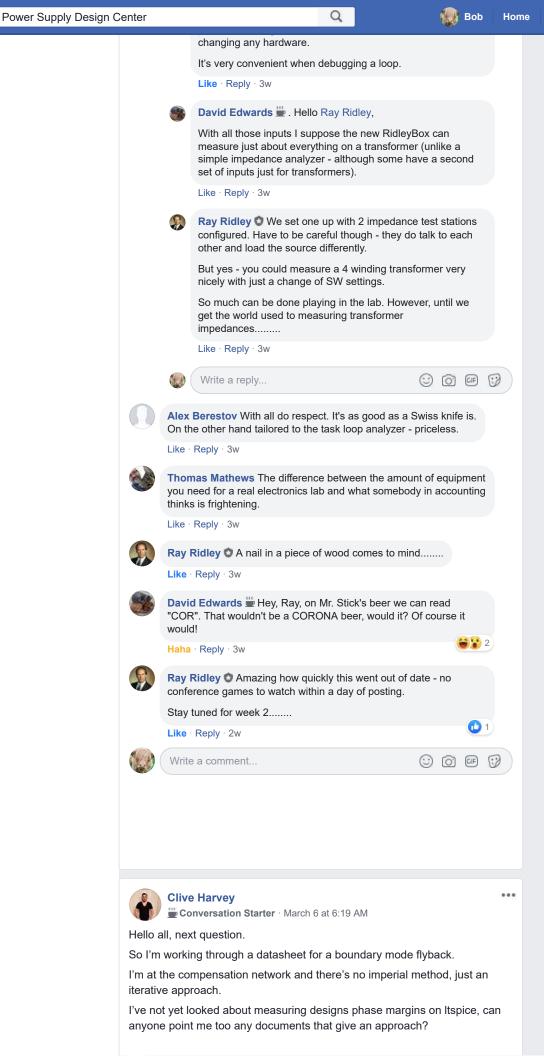
Like · Reply · 3w

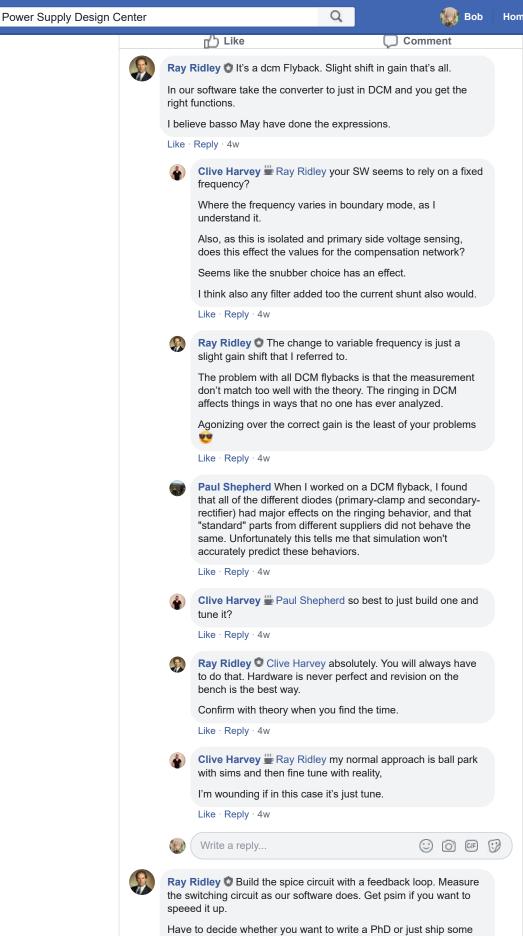


David Sands Ray Ridley Sure looks like it. If only I hadn't just purchased a Keysight scope 🙂

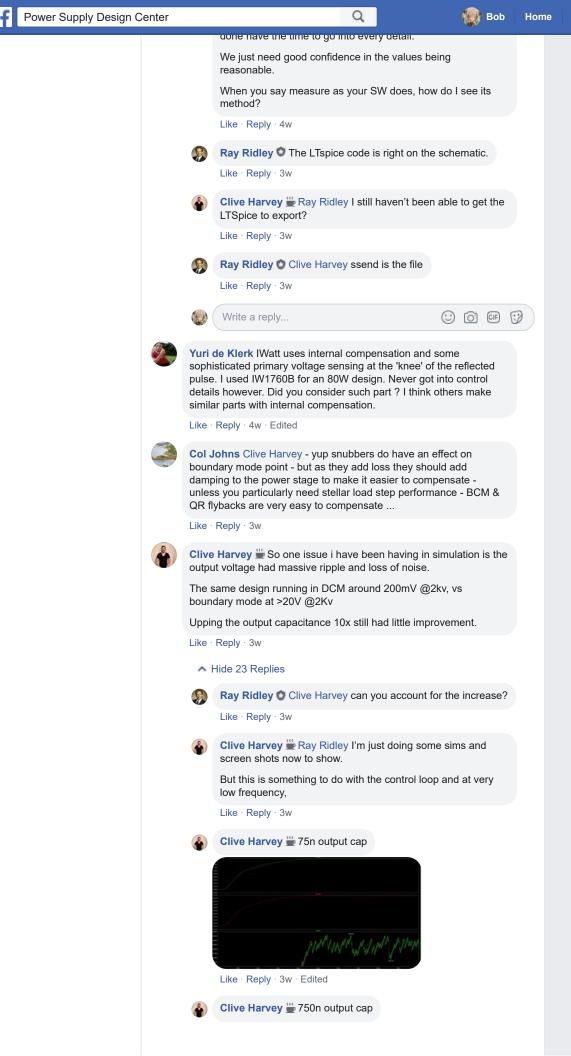
Any examples of where a 4 channel FRA comes in handy? Used the AP300 at my previous workplace but mostly for checking current mode bandwidth on buck converters...







Have to decide whether you want to write a PhD or just ship some rugged product.





Like · Reply · 3w



Clive Harvey as we can see the peak to peak at 75n is around 9V an at 750n is around 30V.

Q

Like · Reply · 3w



Col Johns the control is being affected by something - RFI ..? - yes - most likely ...

Like · Reply · 2w



Clive Harvey Col Johns what do you mean by RFI?

Like · Reply · 2w



Col Johns radio frequency interference caused by the power ckt getting into the control ckt - we deal with this A LOT on equipment sent to our lab, which is a "nearly working" design

Like · Reply · 2w



Clive Harvey Col Johns this is an LTSpice simulation though?

Like · Reply · 2w



Col Johns In that case there is some LTSpice produced ringing ( usually at higher pulse width ) affecting the voltage seen by the f/b loop coupled with too high a gain some where in the control ckt...

i.e. o/p diode ringing - is the graph shown at light load ...?

Like · Reply · 2w · Edited



Col Johns Is it a current mode control of the peak pri side switch?

Like · Reply · 2w



Clive Harvey Col Johns this is my concern, Ive tried a few boundary mode controllers and all have some sort of low frequency control issue like this in simulation.

Is this just LTSpice being annoying?

This is a automotive qualified part, I struggle to believe it would have issues like this in real life?

The design process isn't complicated enough for me to have somehow got the values that wrong.

Like · Reply · 2w



Col Johns Most likely LTSpice playing up yes - without seeing the ckt and the voltages at the various nodes - definite statements are hard to make. In spice though - lots of snubbers are a good idea to make it behave stably ...

Like · Reply · 2w



Clive Harvey Col Johns I posted a screen shot of the circuit. What I have there is the test fixture with tweaked values.

Like · Reply · 2w



Col Johns Sorry I have not seen that screen shot ...

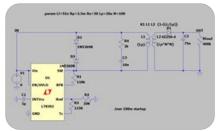
Like · Reply · 2w



Clive Harvey well It doesn't seem too have uploaded, I'll attach







Like · Reply · 2w

Col Johns If the PIV is exceeded on the o/p diode it will break down in spice just as per the real world - and cause issues - a wee bit of filtering RC on the FB pin seems sensible too.

Like · Reply · 2w · Edited



Clive Harvey Col Johns ok, I'll take a look at that, it's a 4.5kv diode, I'll try upping it.

Like · Reply · 2w



Col Johns For that particular diode - the Trr is 2uS, so I wouldn't run it faster than 5kHz in the real world ... look at the currents in the diode and the Tx pri... also with a 1:100 turns ratio you only have 20V of flyback volts on the pri side - this means the diode will see 900V at turn on - for 9V vin plus 2kV of Vout plus any spikes ...!

Like · Reply · 2w · Edited



Clive Harvey Col Johns the real world diode I'm using is the 2x series R5000F but now I look for it, the datasheet doesn't give a Trr, I wonder if I've given myself an issue here?

Like · Reply · 2w



Christopher Richardson Hi Clive Harvey, if you have a contact at Analog Devices, ask them for information about performing Bode plot analysis in LTspice. I worked as a Linear Tech-dedicated FAE at Arrow for a few years, and I helped update the section of the LTspice seminar dealing with this. It takes a long time because the software has to run a sim for each frequency point, but it can be done. Hope that helps!

Like · Reply · 2w



Clive Harvey Christopher Richardson would this be to plot the control loop response to a single in the feedback path?

With this particular controller I'm not sure how easy that would be too do.

Like · Reply · 2w



Write a reply..



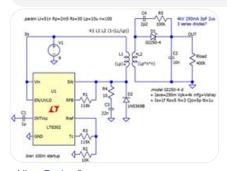






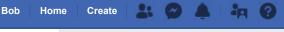
#### David Edwards . Hello Clive Harvey,

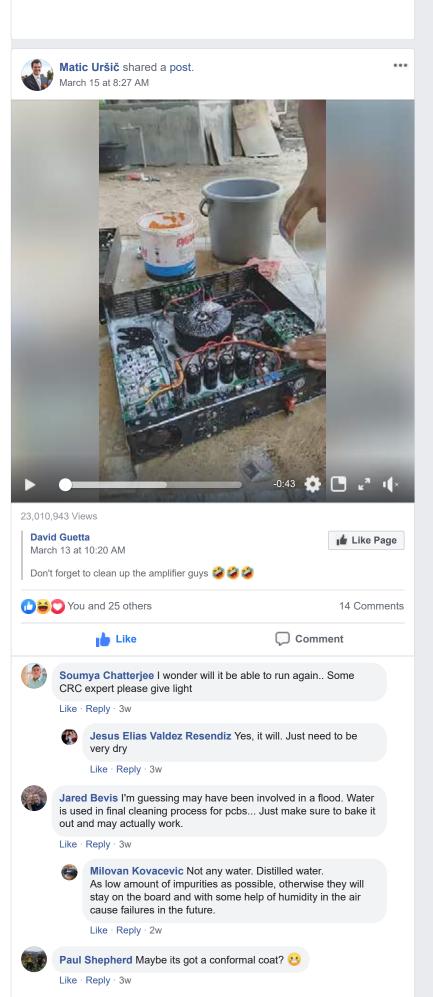
Perhaps your transformer inductance is too high. Also you need RC snubbers across the switches (IC SW and output diode), not across the transformer.

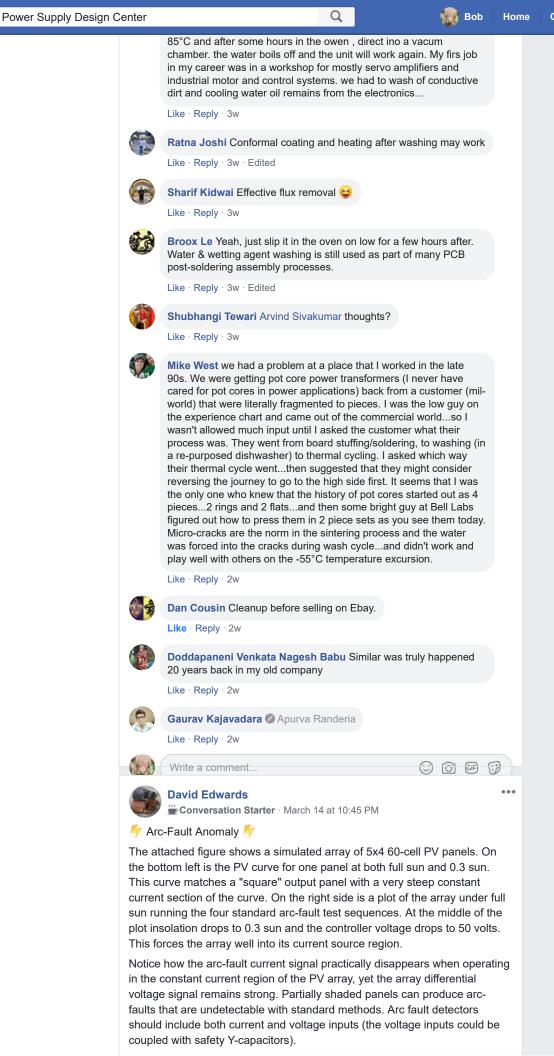


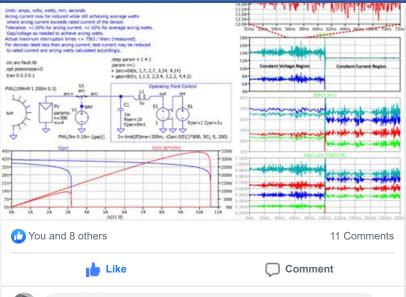
Like · Reply · 2w

Q









Q



**David Edwards** This anomaly is not just theoretical. I have verified this detector "blind spot" in the lab with our PV array and an actual arc-fault.

The arc model uses a physics based negative incremental resistance arc model. Arc voltage and current are both affected by gap length. The model varies gap length chaotically about the nominal.

Like · Reply · 3w



David Edwards Many group members have designed or worked with photovoltaic power conversion systems. Many of these are prone to unmitigated arc-faults because they create high voltage dc with a current source characteristic when shorted. PV panels are powered by the sun so they are difficult to "turn off." For these and other reasons arc-fault physics, detection and safe interruption is of interest to many power conversion engineers.

UL 1699B is the controlling standard in the USA for arc-fault detection and interruption, but the field is in its infancy and the standards, test methods and mitigation requirements are continually evolving.





Sanchit Mishra I had a question. Partial shading can be a fast phenomenon (milliseconds) while arc testing is significantly slower detection (seconds). Doesn't that eliminate this?

I always thought the worst case "non detection" was panel to panel arcs which goes undetected as you don't measure all the inter-panel currents or voltages, thus have no information about what is going on. Didn't assume partial shading caused any major issues due to the difference in time spans of shading vs detection.





make some arcino much narger to detect, wany cases of partial shading can be long duration (bird droppings, leaves, etc.).

Most arc-fault detectors only target series arcs inline with the main power path. Parallel arcs to grounded metal are another phenomenon altogether and may be undetectable by some series arc-fault detectors.

PV system safety evolved from when panel voltage was just above the battery (12V or 24V) and charging was controlled with a relay switch. Significant arcing was not possible in those low voltage systems and shock hazards were low, so the only safety measure was a one amp ground fault detector.

Like · Reply · 2w



Brian Faley I've worked with three IC manufacturers who were all targeting developing a chip to do the heavy lifting of accurate arc fault detection. Unfortunately, they all abandoned the market, because the standards are ill defined and changing, pretty much blind to parallel arcs, and the liability issues drove them all to abandon the efforts. So David Edwards, what have you come up with to solve the parallel issue? Series is possible, especially if the detector lives on the roof near the panels. It's not as prone to the attenuation issues. In my opinion, any solution requires measuring current and voltage, it's all about the energy, and that means simple solutions aren't going to have the horsepower to do the math.

Like · Reply · 2w



David Edwards . Hello Brian Faley,

I don't have a general solution (only a series arc detection solution for a specific product - and the company from which I retired was unwilling to pay to have it tested and certified). Regarding parallel arcs - never worked that problem.

What I do know is that the incremental resistance of a panel can vary (depending on operating point) to where sensing for chaotic current becomes useless in a panel's constant current region. This has been completely overlooked and is why voltage (or perhaps power) sensing is needed at the panel level. All it would require is a differential voltage signal coupled through safety Y-caps summed in with the existing current sense, yet nobody is offering this.

I've developed a very accurate LTspice of an arc (difficult) and an array (easy), so testing out ideas is easy, but there is little motivation to do so.

Like · Reply · 2w



Brian Faley I've been through the arc fault certification gauntlet three times, and I have to say I think it's a racket. Each NRTL had their own take on the requirements, and were more than happy for us to spend money teaching them about how to conduct the tests, and everyone required more tests than were in the standard. Biggest gotcha was the arc fault board we purchased from the company that bought my former company was only tested to radiated emissions at 5kV per meter when the test of the inverter required 15kV per meter. That was fun.

Like · Reply · 2w

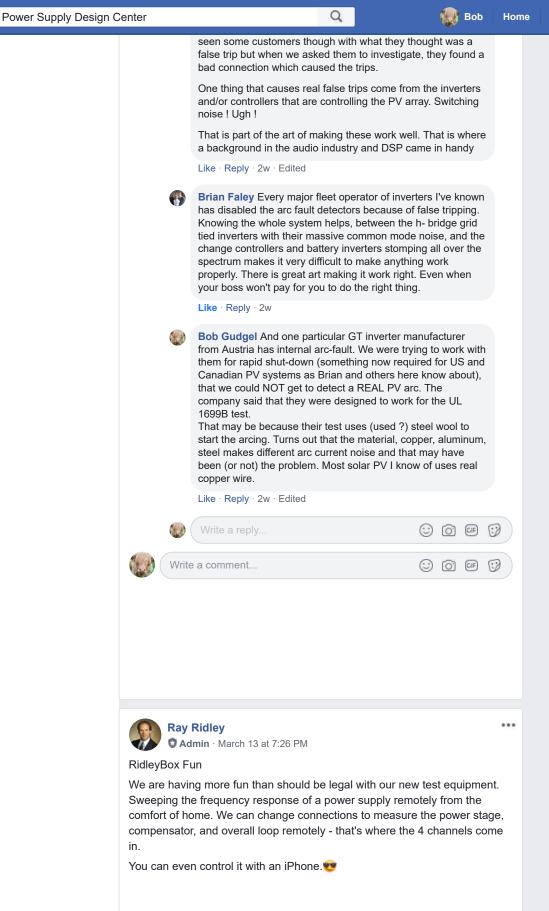


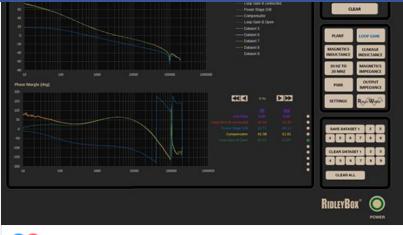
Bob Gudgel You BET that NRTL's are a racket! The Mafia as someone near to me analogizes.

As for parallel arcs, a few years ago now, we (MidNite Solar) worked on that more or less successfully. For the simple case, series arc, you open up the system and parallel arcs, you short.

Another engineer and I went to Sandia Labs where they wanted to test the system which worked well in that scenario. Inside the array parallel arcs as well.

https://energy.sandia.gov/.../SAND2013-5916...





Q



🚹 🔼 Jay Philippbar, Brian Faley and 32 others

22 Comments



r∆ Like



Comment



Ray Ridley O I wish I had this capability when just starting out on my career. The next generation are going to be spoiled.

We asked conference attendees what they wanted most on a new analyzer and the young ones all really wanted to be able to run tests remotely.

The next generation of analyzers is all about ease of use and the software.

And yes, you can do all this with the AP310 as well. (Not the 4 channels though).

Like · Reply · 3w



Broox Le Sounds handy for software defined digital controllers where the control designer could be remotely working on the digital code tweaks and retesting the responses.

Like · Reply · 3w



Ray Ridley V Its pretty timely for this age of working remotely in one way or another.

Like · Reply · 3w



Alex Berestov So one have to buy i device to have an operational unit

Like · Reply · 3w



Paul Shepherd Alex Berestov I don't think it's required, but wireless connections do generate less conducted noise!

Like · Reply · 3w



Ray Ridley 1 Its an option, not a requirement.

Like · Reply · 3w



Alex Berestov Just kidding. I would love to get such a box.

Like · Reply · 3w



Write a reply...











Paul Shepherd Very exciting! Is there an official release date? Data sheet/manual reveal date?

Like · Reply · 3w

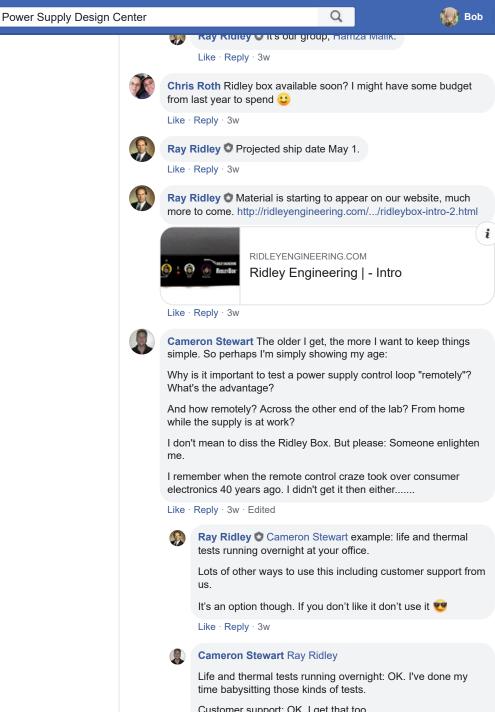


Hamza Malik I thought we couldn't market stuff in this group 🤔

Like · Reply · 3w



Hamza Malik Although i must say, this is something really useful



Customer support: OK, I get that too.

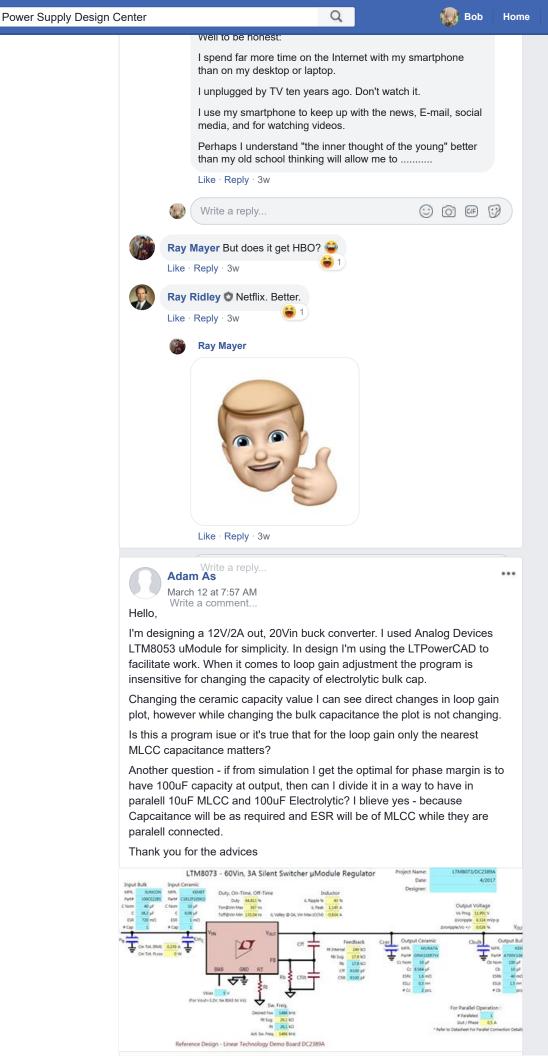
Perhaps it's changing demographic preferences that I'm trying to understand. The "Young Engineers" you've mentioned: What's their motivation?

Like · Reply · 3w · Edited

Ray Ridley Cameron Stewart no idea. We just asked them last year at apec what features they really wanted.

iPhone control was high on the list for several of them

I can't help you with the inner thoughts of the young though if that is what you are asking 😎







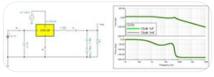


Pablo Roberto Oliva you have to specify de # of pcs, is the last row

Like · Reply · 3w



Nicola Rosano It is correct. If you're looking at the control to output transfer function, the input is virtually grounded' Then the Bulk cap is shorted (not visible). That cap by the way has huge impact on the input filter, as it alters Zin. If you use Vorperian approach you see



Like · Reply · 3w · Edited



Alain Laprade I disagree. The bulk cap is always visible in a control-output transfer function, irrespective of whether it is voltage mode or current mode.

Like · Reply · 3w · Edited



Ray Ridley O Confusion over which cap is called the "bulk" cap, I think.

Like · Reply · 3w



Alain Laprade "Another question" unclear to me. You may want to clarify. A parallel combination of ceramic/electrolytic is of course desirable. As to the influence of the bulk, the 40 mOhm ESR may be dominant (left hand plane zero). The bulk ESR will help with your phase margin, but do be cautious as to simulate the min/max values from temperature dependence to avoid surprises in the field.

Like · Reply · 3w



Ray Ridley Sounds like you just volunteered to look into this, Alain Laprade.

Like · Reply · 3w



Alain Laprade Ray Ridley Doooh! 63

Like · Reply · See Translation · 3w · Edited



Ray Ridley Dets be clear here. I think he is referring to the output cap Cbulk on the schematic. That should absolutely affect the transfer functions.

He is no talking about the input bulk cap. That will have no effect on the schematic shown since it is shorted by a voltage source.

In the real world, it will change things since there will be inductance between the input source and the cap, ie an input filter and Nicola Rosano has quite correctly pointed out.

Like · Reply · 3w

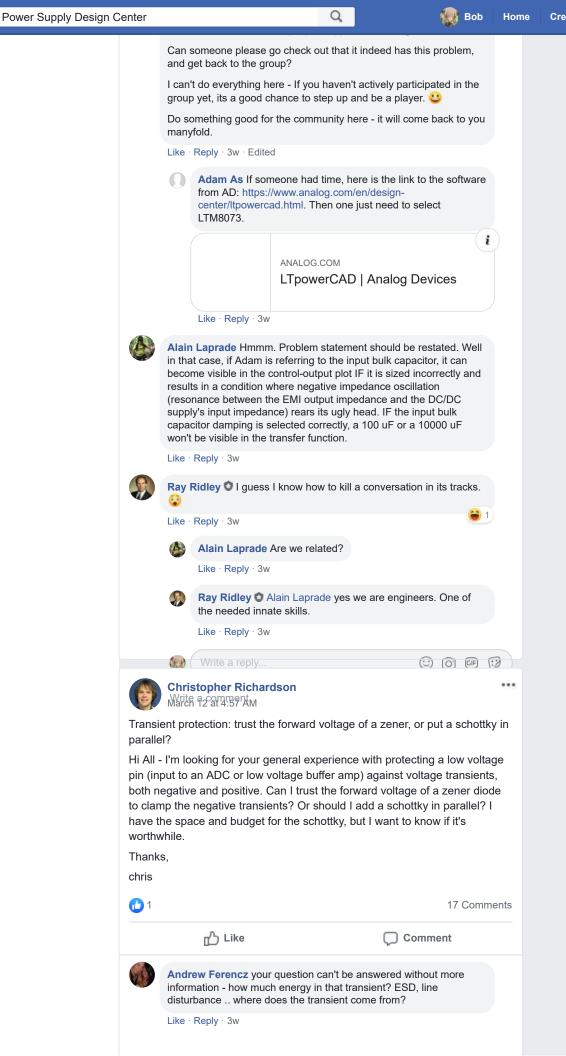


Nicola Rosano Honestly I have never called Cout (or Cfilter) = Cbulk. My fault if Alain Laprade was referring to that one. Obviously if Cout changes all transfer functions change: control 2 output, line 2 output and Zout and less intuitive Zin as well.

Like · Reply · 3w · Edited



Adam As Yeah, I ment the output electrolytic saying 'bulk'





withstand voltages are in -0.3V range. You can check from datasheet.

Like · Reply · 3w



**Stuart Wood** I prefer clamping schottky diodes to the rails like Akif Hakkı Polat said.

Like · Reply · 3w · Edited



**Oliver Sedlacek** Speed matters. Zeners are very reliable to the extent that they are trusted by authorities to form intrinsically safe barriers, but they are a bit slow for some applications.

Like · Reply · 3w



**Stuart Wood** Low voltage Zener diodes have very large junction capacitance that can interfere with signal integrity.

Like · Reply · 3w



 $\begin{tabular}{ll} \textbf{Kadir Yilmaz} Forget zener use two Schottky diode . One from ground to sense , the other from sense to ic supply voltage \\ \end{tabular}$ 

Like · Reply · 3w · Edited



**Broox Le** For an analog input line, I prefer schottky clamps to the rails; I only use zeners or tvs when I don't have a rail voltage to clamp to or to prevent overvoltage on the rail.

Like · Reply · 3w



Arief Noor Rahman See Agree...

Like · Reply · 3w



Richard Payne Broox Le yep

 $\text{Like} \cdot \text{Reply} \cdot 3w$ 



Brian Faley Schottky diodes are fine for some signals, but beware the high leakage current at elevated temperatures on sensitive signals, and stay within the pulse current ratings. Also, the practice of using the power supply rails as a clamp-to voltage assumes the rail has the capacity to absorb the transient. Many LDO regulators don't like being back fed and lack reverse current protection diodes leading to a big voltage spike. Know your power supply. All depends on the amount of energy.

Like · Reply · 3w



Nathan Ellis Brian Faley good point. Would think you could mitigate this by just adding more decoupling capacitance to catch excess energy while keeping voltage low.

 $Like \cdot Reply \cdot 3w$ 



**Brian Faley** Completely depends upon the amount of energy. This is a pretty classic problem where the solution has to address the problem statement. Prescriptive solutions are a dime a dozen. Be sure you know the side effects.

Like · Reply · 3w

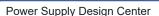


Charlie Elliott 
■ Bat54s and RC for noise filter + swapmping S+H internal cap + helps with ESD and BCI etc.

Like · Reply · 3w



Charlie Elliott ∰ But as others have said, watch out for high temp leakage if high impedance node. Can be mitigated by using much higher voltage part than you need to some degree.







ome

2







aborbed? What is the amplitude and duration? How much energy before the clamp fails? are you putting in a series impedance to help with the peak energy issues?

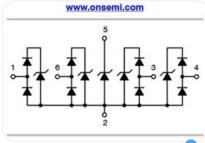
Transorbs and TVS parts can be big and bulky. A simple small zener might look good on a schematic but its not much use if it gets zapped by the first pulse that comes along.

Look at a good production power supply. There you will find good, well researched data with years of experience behind the design decisions.

Like · Reply · 3w



Alex Berestov A little bit of both. For instance: NUP4114. Cheers



Like · Reply · 3w · Edited





Christopher Richardson Wow, what a mix of emotions! First, as usual, all of your suggestions and ideas are both excellent and helpful. I hadn't even considered a second schottky to +VCC, I don't think I ever saw this done, or if I did, I didn't realize what it was for. On the other hand - I'm a bit embarrassed for not thinking of it. This forum is wonderful. To answer the questions, this input is the tap of a resistor divider for an electronic load, and I myself connect the DUT



# Atish Tailor March 10 at 2:50 PM

Dear experts.

I am doing some research in trying to understand the DC-DC converter used inside a Tesla powerwall.

I have made a bit of a guess as to what the basic internal blocks are.

On the HV side, the voltage variation is 350-550VDC.

On the LV side it charges a 48V nominal battery. This is a 5kW bidirectional converter

This can't be a buck or boost variant converter as the conversion ratio is 13. This must be a topology with a transformer.

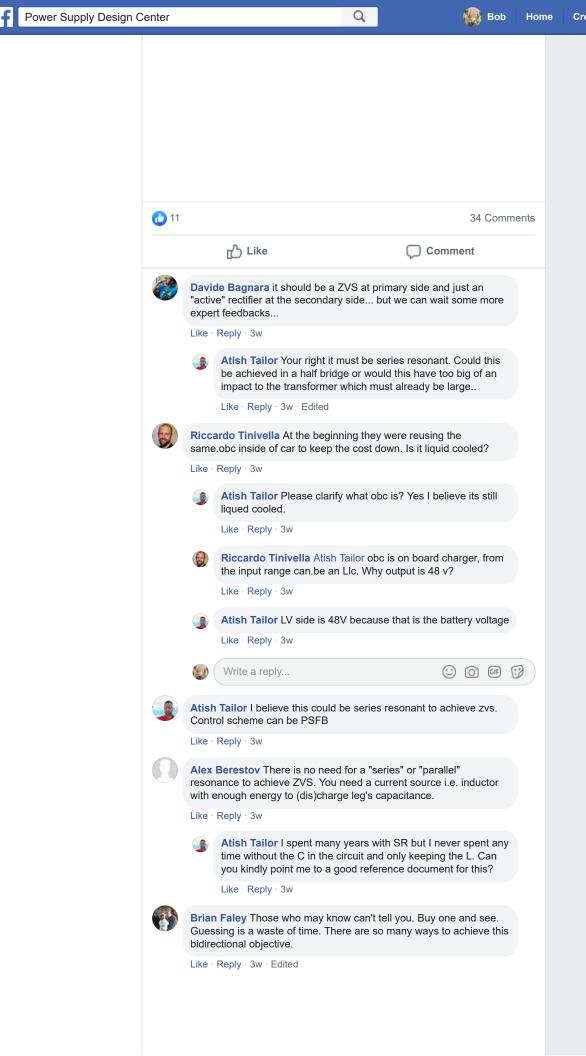
It is possible this could be 2 sets of Hbridges with a transformer in the middle as this would support Bidirectional DC power flow.

It could also be a half bridge on the LV side and a full bridge on the HV side as shown in second immage (save 2 mosfets).

Are there any other ideas as to the topology that could be a good idea provide upper 90% efficiency?

Maybe someone knows what's inside the Powerwall?

Many thanks for your comments in advance.



would be definitely up for it. I disagree with you b guessing can put options on the table and lead to the right solution. It's all part of the learning we do every day and we are all init together.

Like · Reply · 3w



Brian Faley I think they initially adopted the 48V nominal battery voltage to duck under US NEC2014 household installation codes for battery systems, and because they were planning on the HVDC being connected to a standard transformerless grid tied PV Inverter it necessitated galvanic isolation on the battery side - to do otherwise would have been prohibitively costly because of all the cells requiring reinforced insulation between the cell and heat exchanger. They chose to implement a deadbanded droop control method of power transfer to make it compatible with PV inverters - surplus PV gets stored, and then used when the voltage falls low enough to trigger a discharge. The battery pack was adopted initially from a car - including the liquid cooling which requires an auxiliary isolated power supply for the circulation pump and battery heater, and internal electronics. Their gen 2 contains an inverter as well. Two huge things drive the power electronic choices: 1) COST, 2) Efficiency. All of these things are not guesses - they are observations from tear-downs, user documentation, and close study of regulatory requirements. I'd be surprised if the DC/DC converter efficiency is lower than 96%.

Like · Reply · 3w · Edited



Atish Tailor I cant understand why isolation would be a requirement? They could have made the enclosure out of plastic and said it's doubly insulated and no userservicable parts inside..

In the above case if the user was to use in a DC transformerless system, why are the solar panels allowed to be non isolated and the powerwall suddenly needs isolation?

You are correct we can estimate (or guess as I call it) the DC-DC is at 96% because overall its spec sais its 92%. This implies its 96% for charging and 96% for discharging plus some auxiliary power consumption brings it to 92.

I there appears to be no teardown immages and videos.

Like · Reply · 3w

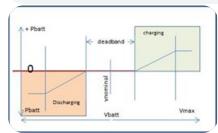


Atish Tailor Also what is deadbanded droop control? Kindly?

Like · Reply · 3w



Brian Faley See graph - for deadband droop control. It's widely used in DC microgrids. A variation is used for Freq/Watt protocols in AC grid distributed energy resources -DER.



Like · Reply · 3w



Atish Tailor Oh yes the dead band. This is controlled using 2 pins one that controls the direction and the other controls the power. The decision is made based on the measure of a ct at the incoming grid feed and optionally a timer based system. I hope iv not left or overlooked anything.













battery conversion.

I ended up mating a Weinberg Push-Pull converter on the low voltage battery side with a full bridge on the high voltage side.

The high voltage side required IGBT's so the internal body diodes could also be used as rectifiers.

The low voltage battery side required MOSFETs bypassed with schottky diodes as rectifiers.

There were two control circuits. An external transfer control determined which control circuit operated and which way power would flow.

Nothing ZVS or ZCS here and no synchronous rectification. The concept was to keep it simple with ordinary hard switching.

The design concept never made it passed the initial proposal stage so I never got to build actual hardware to make it work.

Maybe someday ......

Like · Reply · 3w · Edited



**Atish Tailor** Interesting concept to keep it simple. It would have been interesting to think what sort of efficiency this could be got upto..

Like · Reply · 3w



Cameron Stewart Atish Tailor

92% is quite feasible.

Like · Reply · 3w



Atish Tailor 92% charging and 92% discharging takes it down to about 84% overall thats the trouble.. if it was 84% and getting rid of lots of power components it would be ok maybe.. but if @84% it only makes the designers life easier, it's a hard one to sell in this day and age..

Like · Reply · 3w



#### Cameron Stewart Atish Tailor

So you need another 3% efficiency each way: 95% charging / 95% discharging for a total of 90%.

You probably need to either:

- A) Run a computer simulation to get a better estimate of losses
- B) Build actual hardware and test.

Once you get something working, then you can take the next step: Optimization.

Maybe that means adding the synchronous rectifiers, and regenerative snubbers on the push-pull Weinberg, or migrating toward ZVS resonant on the full bridge side, or substuting Silicon Carbide Mosfets for the IGBT's.

And maybe it means doing all of the above.

My 92% number is simply an estimate of the minimum baseline performance you can get without optimization.

You need to start out simple and get something working first. Then work incrementally on the efficiency problem.

Like · Reply · 3w



Atish Tailor Some very nice advice there Cameron Stewart much appreciated. You remind me of a really humble gem that trained me and taught me what I know today.. Thank you.

Like · Reply · 3w · Edited



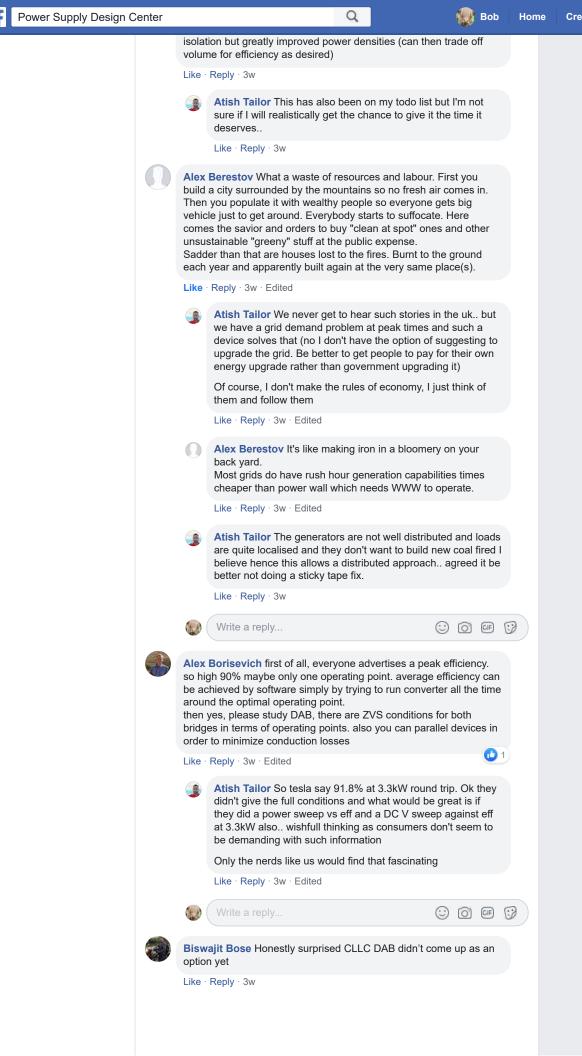


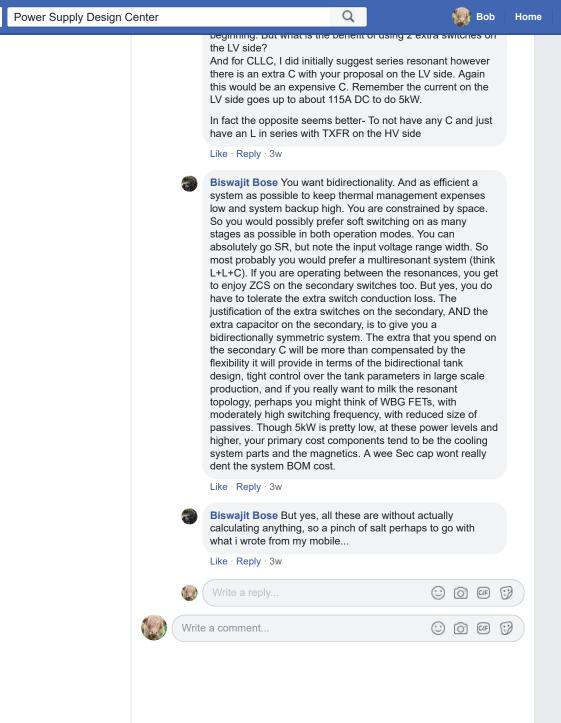














Hello Everyone. This is a great community where I was able to find lots of answers to my doubts. I'm currently facing a challenge with buck converter, and battery. A typical self-made charging circuit.

How can we protect our dc dc converters from reverse current?

I know that reverse voltage (polarity) protection can be achieved using a MOSFET connect in the ground path or live path just before the battery to prevent reverse current flow when connected in reverse polarity.

Q

Home

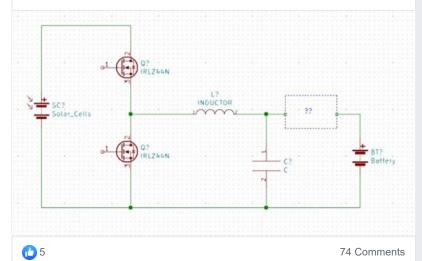
current flowing from battery to the converter. The situation becomes worse when we connect a sync buck when the lower MOSFET conducts and blows itself. How can we prevent that from happening. Some of you may say connecting diode is a solution but it reduces the efficiency even if it is a schottky diode because load current is more than 20A which approximates to around 14W loss across diode and is enough to blow diode off because of thermal runaway and 14W loss is unacceptable in the application.

Please help me getting a concrete solution.

P.S. To make situation even more complicated, the source is a solar panel which means the input voltage is not at all constant and during evenings, above problems occur.

### **UPDATE** -

Below is the schematic for reference.









Janamejaya Rox Have you done any simulation at all?. Schematic or block diagram would be helpful. Very difficult to visualise the problem without it.

Like · Reply · 3w



Sai Prasad I tried on real hardware and faced the above issue. I've updated the post with a schematic

Like · Reply · 3w



Yassir Nadir Have you tried back to back FET for reverse current protection?

Like · Reply · 3w



Sai Prasad That does not work as the fet would already be on. You cannot control the flow of current with that. The back to back FET is used to block current that flows through the body diode of the FET, as far as i know. In my case, The reverse current shouldn't flow.

Like · Reply · 3w



Bob Gudgel Back to back FETs is one way to prevent reverse voltage. So is a relay in the battery positive to the inductor. Those two methods are exactly what the industry uses for this in PV to battery MPPT chargers

Like · Reply · 3w · Edited



Jared Bevis This is usually accomplished through the use of an ideal diode circuit at the output of the power supply. There are many inexpensive controllers out there for this purpose.

Like · Reply · 3w · Edited



**Bob White This^^^** 

Home



kam wonan This seems to be a typical wiPPT Charge Controlle Circuit with Synchronous Buck Converter. A additional Reverse Blocking diode or Mosfet in series to Solar Panel (SPV) is required to prevent SPV Reverse. The Freewheeling Mosfet is more efficient than the Diode. If the timing signal for Top & Bottom Mosfet is proper, then there will be no issues of Cross-conduction. Used this Circuit for upto 3KW MPPT Conversion. For higher Efficiency dual interleaved is recommended.

Like · Reply · 3w

Hide 18 Replies



Sai Prasad Thanks Ram for your comment. I already have implemented the Protection at the SPV side. The problem is at the load side.

Like · Reply · 3w



Ram Mohan Sorry but i could not understand the Load side issue you are having. Please elaborate?

Like · Reply · 3w



Sai Prasad The issue is when the panel power drops, the voltage couldnot be maintained at the load end, so the battery starts to have higher voltage than the converter output due to which, reverse current starts flowing from battery to buck converter itself. That causes the lower side mosfet to short battery terminals and blows itself off.

Like · Reply · 3w



Ram Mohan Sai Prasad have you tried building the circuit or done simulation? The lower Mosfet is turned "ON" only for freewheeling the Inductor Current during off time. The Battery Current irrespective of the Voltage will not flow in "reverse" due to the Inductor.

Like · Reply · 3w



Sai Prasad Ram Mohan I have tested on the hardware. The lower mosfet keeps blowing up

Like · Reply · 3w



Ram Mohan Sai Prasad You need to give more Inputs. What is the Mosfet rating & Gate Driver configuration? How are you generating the PWM? Have you implemented PID algorythm? Please post more details so that it helps every one to solve or learn.

Like · Reply · 3w



Ram Mohan Also post how the Gate drive wave forms of Top & Bottom Mosfet looks like

Like · Reply · 3w



Sai Prasad The MOSFET is IRF3205 N Channel type, gate driver is IRS2110S (smd). I have implemented the controller using Atmel Atmega32.

Like · Reply · 3w



Ram Mohan Sai Prasad The Gate Waveform for Top & Bottom should be some thing like this.



Like · Reply · 3w · Edited





Atish Tailor It would be simpler to to have a voltage detector and if the sc V is > BT V, you start generating your gate drives. Slow ramp as at some point the V at the sc may drop again. Maybe you can get this to work in burst mode

Like · Reply · 3w

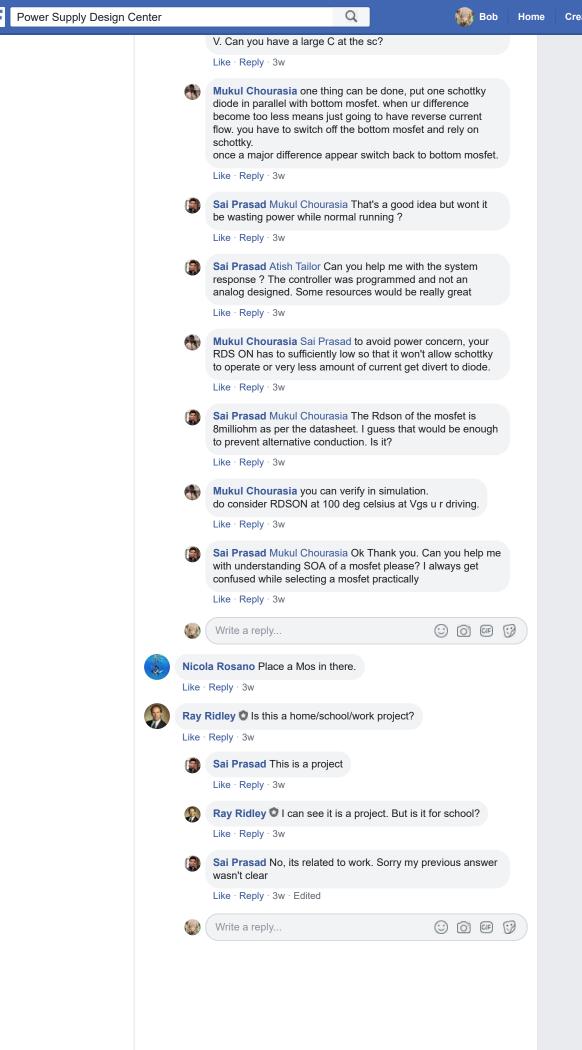


Mukul Chourasia as Atish Tailor told it will be better to sense the source and load voltage and accordingly decide the gate pulses.

Like · Reply · 3w



Sai Prasad Atish Tailor Mukul Chourasia I was trying to do that but within that short period of time, MOSFET blows off



applied to the solar cells, they can enter "stall" mode, and their output will be severely limited until that overload is removed and the cell can reset. This is what an MPPT controller does (no, it is not meant "track" or tilt the solar cell, it is mean to prevent start-up overload, and then to "track" the most efficient load point the cell(s) can handle). In this version, if you cannot integrate proper MPPT control, at least place a diode in series with the solar cells making their output one way, and place a capacitor across the solar cells after that, to allow voltage to build before the choppers switch on.



Ray Ridley Vou need to sense the current and control it. You might not be able to do that with the solution you have chosen, so you have to add circuitry to do that.

Like · Reply · 3w

Hide 14 Replies



Sai Prasad I've actually shown only the concerned part. I included current sensor and all the auxiliary circuit needed for the operation.

Like · Reply · 3w



Sai Prasad The circuit is oversimplified in the screenshot

Like · Reply · 3w



Ray Ridley Well if you have all the current and voltage information should be easy to control as needed when things move in the wrong direction.

Like · Reply · 3w



Sai Prasad True. But within the time of action things are going wrong. The controller implemented is more of a bang bang type. So I was thinking of a solution where the current would flow in one direction like a diode (but not diode) implemented using MOSFETs. I don't know if that exist.

Like · Reply · 3w



Sai Prasad I'm a rookie in control system world

Like · Reply · 3w



Ray Ridley I might suggest changing your controller. That is not where these designs should start. You have to define the functions and protections you need first, then find the controller that gives you what you need.

Like · Reply · 3w



Sai Prasad It was done like that only but I think something is wrong, the response time is slow. I think I should brush up my skills on control system. I did went through some articles from Ridley design Blog. Can you please suggest some resources on practical control system design & analysis and sensing? That would be of a great help. I really need to dive in deep.

Like · Reply · 3w



Ray Ridley Sure. Plan on coming to our workshop. We will get you trained.

Like · Reply · 3w



Sai Prasad Does it happen in India?

Like · Reply · 3w

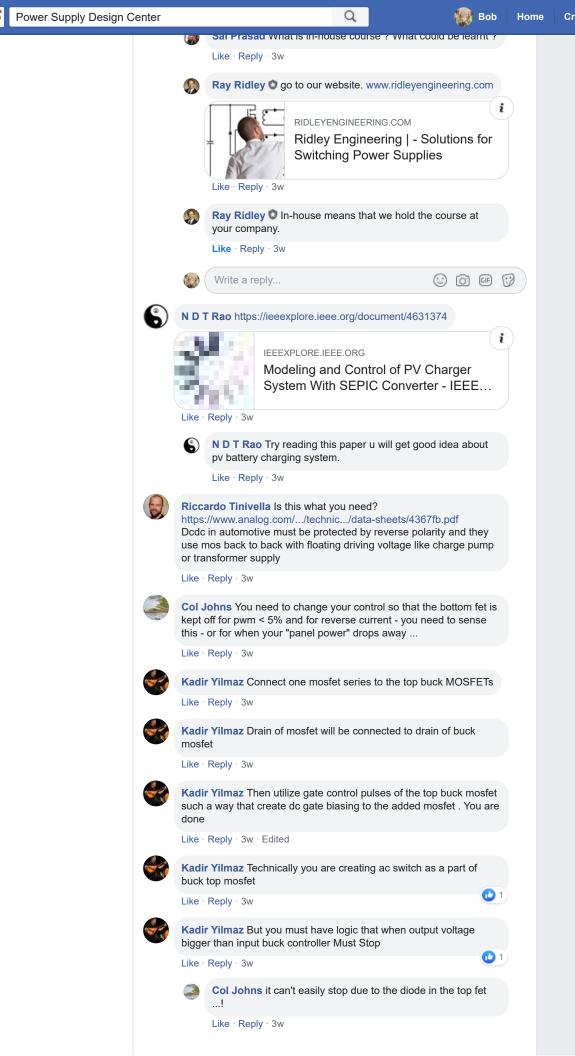


Ray Ridley If you would like to have an in-house course, we can do that.

Like · Reply · 3w



Ray Ridley Otherwise plane fares are cheap to CA I understand.







(1) (a) (c)

Hi everyone,

Write a comment...

I have a problem with a PSFB. It is 800V at input and 825V output. The screen capture below shows the ZV switching on the lagging leg at the nominal load (1450 W, yellow is Vgs, red is Vds and blue is load current ... inverted) but my feedback loop is saturating at full-load (1.8 kW) because of the high value of the resonant inductor (here Lr=145uH!!). The reason for that is the transformer's high parasitic capacitance value (here 500pF). What are your suggestions to bring that cap value lower so I can switch at ZV with a lower Lr.

Thank you



Like · Reply · 3w

# Hide 21 Replies



Lotfi Bgh Ray Ridley you mean by increasing the distance between the two windings?

Like · Reply · 3w



Alain Laprade Lotfi Bgh Interwinding capacitance. Is your inductor winding multilayer or single layer?

Like · Reply · 3w · Edited



Lotfi Bgh Alain Laprade multilayered, but I am afraid there is not much I can do with transformer at the moment since there is not much room left to make any change or dimension increase ...

Like · Reply · 3w



Yuri de Klerk Lotfi Bgh Are you sure the parasitic capacitance is 500pF? (How was it measured?) Did you use clamping diodes? The clamping diodes can be placed such that ZVS gets bad. Is the series cap value high enough? If too low, the energy of the resonant inductor gets eaten by the cap before the transition has even started.

Like · Reply · 3w



Ray Ridley Vuri de Klerk series cap? How about a schematic Lotfi Bgh?

Like · Reply · 3w



Lotfi Bgh Yuri de Klerk I don't see how the clamping diodes can affect the ZVS, if you can give more details on that, thanks. There is a 4uF DC blocking cap, I should probably increase that.

Like · Reply · 3w



Ray Ridley Schematic, please.

Like · Reply · 3w



Ray Ridley Why do you even have a coupling cap?

Like · Reply · 3w



Lotfi Bgh Ray Ridley to a avoid transformer saturation due to umbalcing when voltage mode is used. Some papers evoke this DC blocking cap

Like · Reply · 3w



Ray Ridley Make Cc =



Save you some board space v





Lotfi Bgh Ray Ridley would removing the output filter inductor reduce the overall parasitic cap? Ripple will increase but there is still room to add more caps at the output

Like · Reply · 3w



Ray Ridley Dotfi Bgh That means they gave up on controlling it properly. It is a big part to put back in again, and comes with its own set of issues.

The transformer needs revising in my view. It doesn't necessarily have to get bigger.

Without that, we have a classic and very common situation in power - please fix the circuit, but don't change anything.

Q

#### transformer.

2. I am not looking for solutions than do not include any change, I am just seeking for different solutions.

Like · Reply · 3w · Edited



Ray Ridley You use current mode to balance the transformer. Standard technique.

This solution to this problem must start with the transfomer examination in my professional opinion. That is where we always start. Most problems originate there.

You begin by measuring the open and short circuit impedances. that will tell you much information.

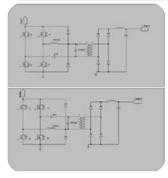
Then you measure the primary to secondary capacitance.

Plan on current mode control with sense transformers.

Like · Reply · 3w



Yuri de Klerk Lotfi Bgh There are two possible locations to put the shim inductor with the diodes. As I can recall putting it near the CD leg takes away some transition energy, especially with high transformer capacitance. Putting it near the AB leg however can result in hot clamping diodes.



Like · Reply · 3w



Alain Laprade Lotfi Bgh Ah, you had stated 'resonant inductor'. I interpreted that statement as it being a separate element from the transformer. As mentioned by Ray, you might have no choice but to revise it.

Like · Reply · 3w



**Lotfi Bgh** Thank you Dr. Ray Ridley. It looks like I still have a lot of work to get it done!!

Like · Reply · 3w



Lotfi Bgh Yuri de Klerk thanks a lot. I haven't tried this yet. I will give it a try.

Like · Reply · 3w



Ray Ridley Here is something to think about. IBM were in preproduction (1000s) and started encountering a failure rate of about 2% during light load tests.

Power supplies are a LOT of fun. Why we sign up to this is a mystery.

Just ship the app note demo board and pray! Move on to your next job quickly in case it gets returned.

Like · Reply · 3w



Yuri de Klerk Ray Ridley is right. For 500pF to (dis)charge from 800V with 145uH you'll need 1.5 Amps (about 1200 Watts?) So 500pF is way too high for making it work a little proper. 145uH at 100kHz is 91 Ohms. Or is your switching frequency 10 times lower?

answer is really about.

Like · Reply · 3w

details. 😎

Ray Ridley that's true. Realize, though, that it is the magnetics mountain that needs climbing. The rest is just





verikat Karthik Are you using an extra resonant inductor or just the leakage of the transformer? What is the Coss of the SiC mosfets?

Like · Reply · 3w



Lotfi Bgh Venkat Karthik thanks for the comment. It is discrete and I see what you mean, I will try some additional caps across the lagging leg mosfets.

Like · Reply · 3w



Ray Ridley How is that schematic coming along? By giving that, you give a little something back to those that are helping and watching. Doesn't have to be complete.

Like · Reply · 3w



**Lotfi Bgh** Ray Ridley I am grateful to this group and I will see if sharing the schematic is something possible.

Like · Reply · 3w



Ray Ridley You've already given the scematic in words. Just put it into pictures. FETS, coupling cap, Lr, transformer, diodes output cap, output L.

Nothing confidential. Just the overall scheme which is public knowledge. They we don't all have to guess about and external inductor, series cap, etc.

Make it easy for people to answer your questions. Much better results that way.

Like · Reply · 3w



Col Johns For this sort of app where you have 500pF of C on the pri wdg ( and the sec too? or is it 500pF combined for pri and sec - as they are fairly closely coupled? ) it is necessary to have lots of commutating energy and extra C across the mosfets to give you slower transition times - say 250nS at least - unless you are going to rewind the Tx to try and get a lot lower C there )

If you do this you will need energy from a commutating choke - these can be additional to the main ckt - we have done this fix to other peoples designs ( luckily there was space ) - it also greatly reduces RFI and switching losses if done right - EMC was what we were originally called in for ... - but then had to fix the power ckt ... and the gate drive ...

Like · Reply · 3w



Lotfi Bgh Col Johns thank you for the comment. Yes, it is pri and sec combined. Adding some caps across the mosfet is supposed to decrease the equivalent parasitic capacitance and I have some margin on the deadtime so I'll give it a try. Yes, it also helps with EMI, even with lower loads. It is always better to have quasi-resonant switching than hard switching.

Like · Reply · 3w



## Snehal Bagawade Hi Lotfi Bgh

In a PSFB why are you adding 145uH series inductor on primary? It may have increased your problems with diodes more. What is the value of filter inductance on the output?

Like · Reply · 3w



**Lotfi Bgh** Hi Snehal Bagawade snubber is doing its job and diodes can take high voltage. But the plan is not to use a 145uH because it is too high. I was expecting something between 15uH and 30uH.

Like · Reply · 3w

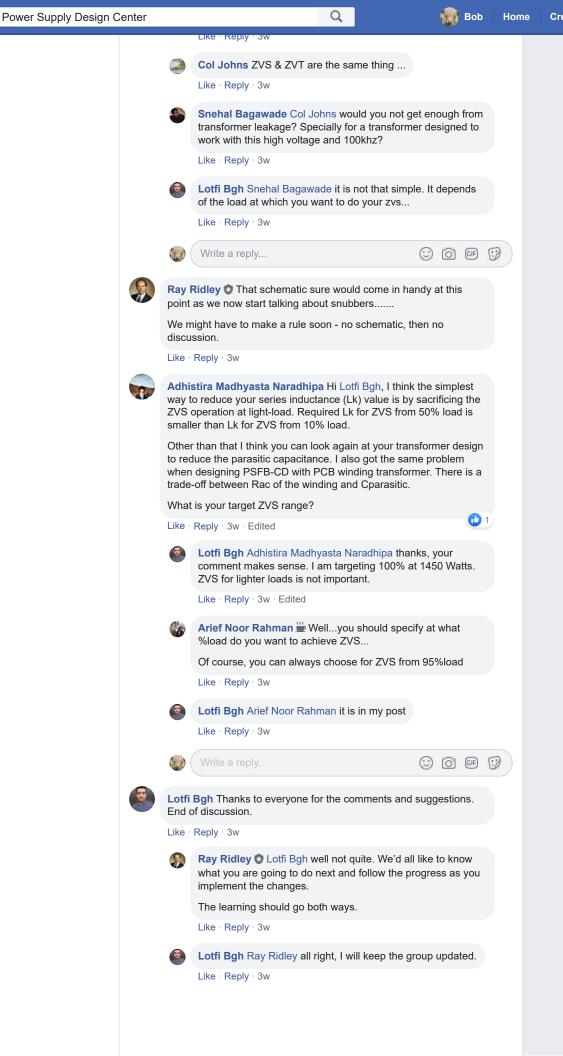


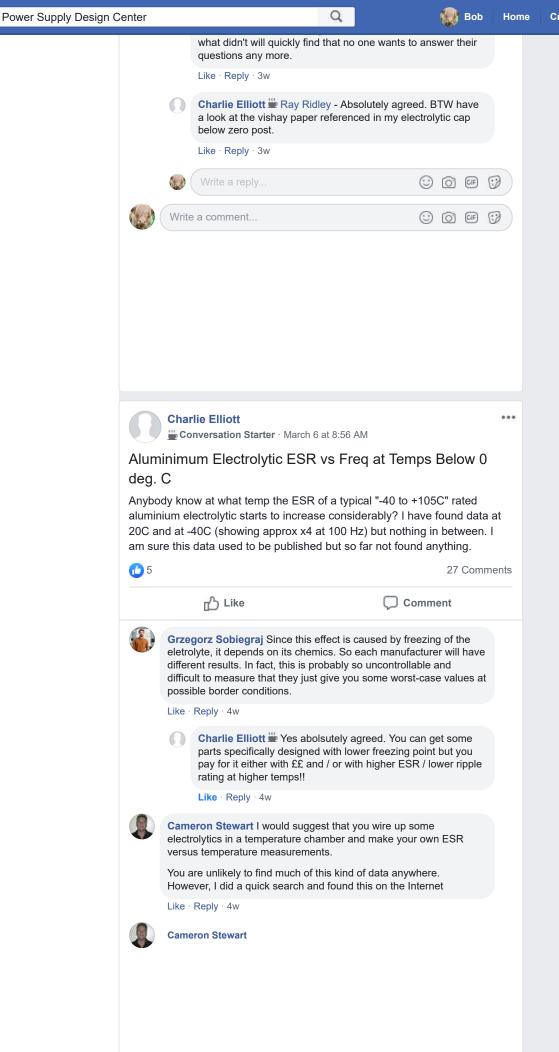
**Snehal Bagawade** My point is that you don't really need an inductor in the primary side. Why do you have it there?

Like · Reply · 3w

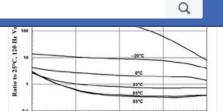


**Col Johns** an inductor is common for phase shift full bridge PSFB ...





Home



Frequency (Hz)

Like · Reply · 4w

Charlie Elliott Cameron Stewart - You must be better at digging than me. Which m/f is that for?

Like · Reply · 4w



#### **Cameron Stewart** Charlie Elliott

This graph was pulled off a paper found on ResearchGate. The manufacturer is anonymous.

Like · Reply · 4w



Cameron Stewart Most of the change occurs between -20C and -40C. In my past experience this temperature range is where an otherwise stable power supply will begin to oscillate or otherwise misbehave.

Like · Reply · 4w



Alain Laprade Make sure you distinguish between solid and liquid Aluminum electrolytic capacitors. Solid types offer better performance. Alternatively, consider Aluminum-Polymer capacitors if the voltage rating is within your needs. Expect to pay more on a per unit basis, but you won't need as many in parallel to compensate for the -40C degradation that liquid aluminum electrolytics have.

Like · Reply · 4w · Edited



Charlie Elliott Alain Laprade - Thanks for the useful comment. For the sorts of thing I am particularly interested in (400V+ and 470uF+) I dont beleive solid electrolytics or hybrid polymers are an option.

Our biggest concern in the application we are looking at (cold soak to -30C and then needs full power immediately available) is the potential reliability implications. Loss will be much higher which will of course heat up the caps but could this thermal shock cause some kind of premature failure?

Like · Reply · 4w · Edited

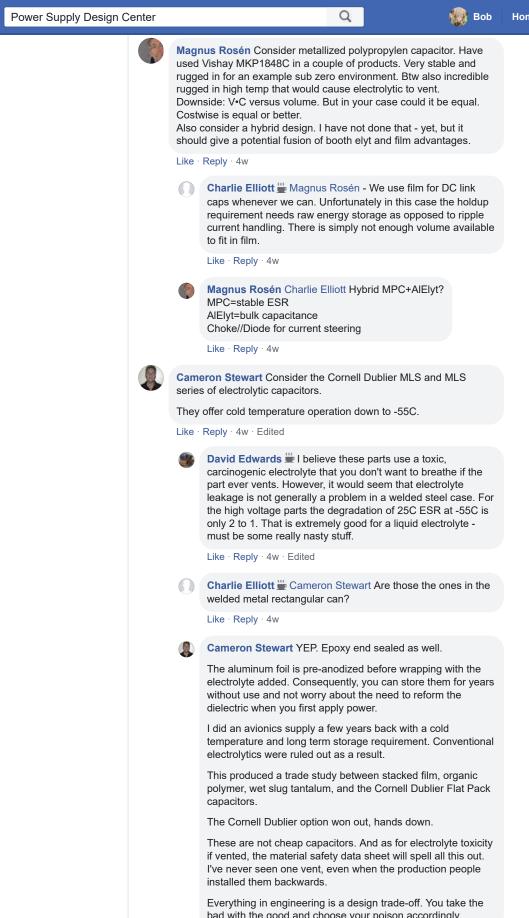


Alain Laprade Charlie Elliott If information isn't available from the datasheet or the manufacturer's reliability information (normally available, but as separate information from the datasheet), I would consult their applications staff for guidance on the failure mode of concern. You do not define your thermal shock operating concern. Others may chime in with different information, but I've never heard of a -30C capacitor thermal shock failure (hot temperature, yes it can happen but that isn't your question). From my own experience, I would be focusing on stability and EMI concerns from the high ESR at -30C. For an input filter, this can reduce the effectiveness of an EMI filter, and also introduce vulnerability to negative impedance oscillation interaction with the downstream DC/whatever converter at low input voltage. If this is an output filter (mentioned by Cameron Stewart above), then the stability of the feedback loop at cold may be of concern as the modulator plot response (control to output) may have a mid-frequency gain increase which voids the intended bandwidth.

Like · Reply · 4w



Charlie Elliott Alain Laprade - In this case I only need to worry about the EMC implications as this is an input filter on a motor drive. I have sent e-mail to a couple of applications engineers last week. I will let everybody know if they come back with anything of interest. I have a horrible feeling I will be told to test it!!



bad with the good and choose your poison accordingly.

Like · Reply · 4w · Edited



Write a reply...



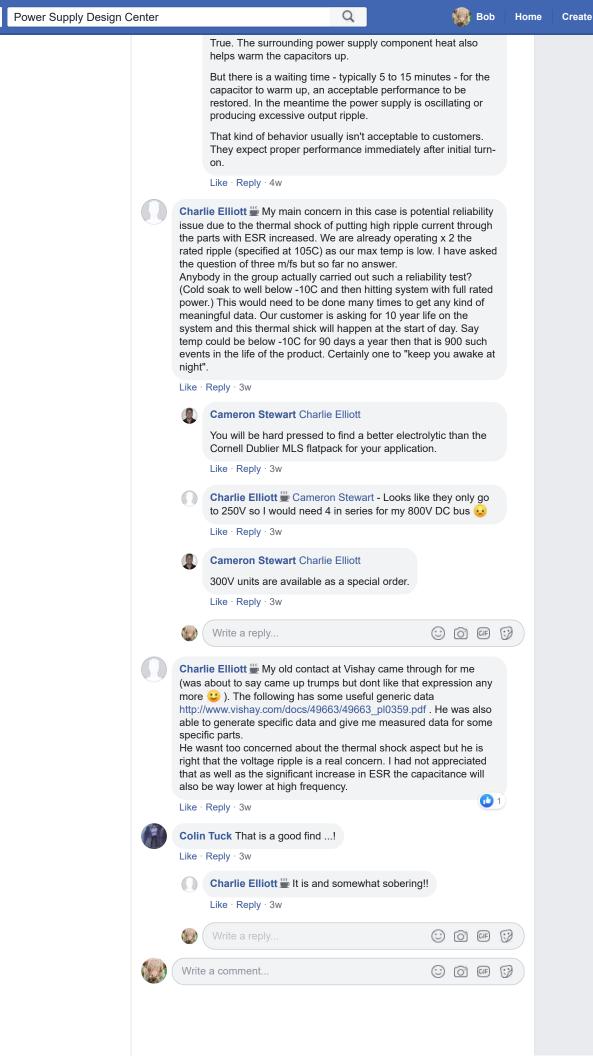


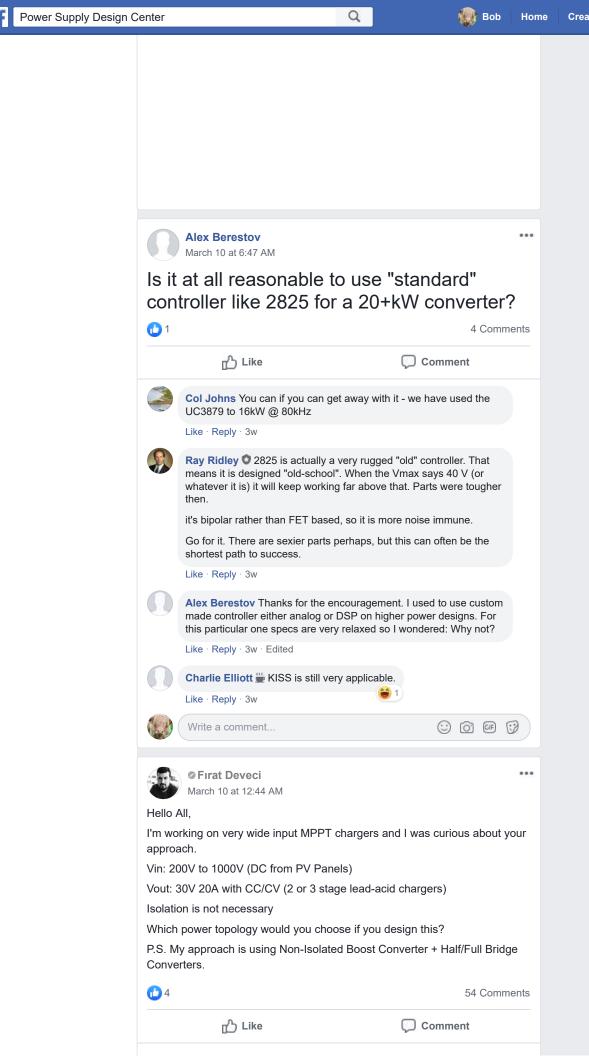






Phil Lane If the ESR was high enough the cap would warm itself





Like · Reply · 3w · Edited

### Hide 12 Replies



Firat Deveci In the field, users generally use solar panel between 600-700V. They don't use these panels for battery chargers, because for 600V voltage level, they have to use around 20 solar panels in series. If every sonal panel power is around 250W, total power will come 10kW. They are generally used for solar water pump in agriculture area.

Like · Reply · 3w · Edited



Edward Ralph That didn't answer the question. I've fitted solar and can't see why you'd want such a wide voltage range. Current changes a lot voltage not so much, relative to pout.

Like · Reply · 3w



Firat Deveci Edward Ralph They want like this, i dont know why, I am designer not a customer, maybe they want to fit more or less series panels and want one converter to use.

Like · Reply · 3w · Edited



Edward Ralph Ahh ok. I was going to say it doesn't sound like an engineers spec!

Like · Reply · 3w



Scott Styles it is always good to challenge requirements. I see this a lot. someone with a statement of what they want you to do, but unfortunately not enough understanding to really know what they need. I guess if you're in a contract design role it is easier to detach yourself from this, but when you have to live with things long term...

Like · Reply · 3w



Scott Styles driven past heaps of these on 4wd trips but never had the opportunity to stop and take a look. i think there's a market here. https://www.trademe.co.nz/.../listing-2569633342.htm...



TRADEME.CO.NZ

**Epump Solar Water Pump** 

i

Like · Reply · 3w



George William Tyler Pirat Deveci watch out for this. if customer wants silly things it is better not to do it!

Like · Reply · 3w



Firat Deveci George William Tyler I know they will use it around 600-800V input ranges. But in the morning or before sunset, PV voltages comes 300-500V and motor drivers dont run the motors. In this situation, they want to use this level to charge batteries especially in the morning.

Like · Reply · 3w



Kadir Yilmaz first that is not true

Like · Reply · 3w



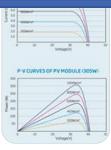
Edward Ralph Pirat Deveci if the voltage is low, no current will flow anyway.

Like · Reply · 3w



Edward Ralph This is what mean, panel voltage doesn't vary much due to sun irradiance.

Home



Like · Reply · 3w



Firat Deveci Edward Ralph you are absolutely right, this is only my thought. I dont know about customer how to use this converter. This is the spect I have to handle.

Q

Like · Reply · 3w



Write a reply...













George William Tyler Firstly, I would probably make it isolated anyway, as to get from 1000v to 20v would be better handled by a transformer than a buck etc. Maybe a boost first with this doing the mppt function? Maybe better to have a buck from 1000 to 200 then DC to DC isolated 200 to 30.

Like · Reply · 3w · Edited



Firat Deveci George William Tyler I want to boost voltage to 800V to make current very small. After that i will use transformer to make it 30V.

Like · Reply · 3w



Petrica Barbieru May try buck only with MPPT conditional by load level.

Like · Reply · 3w



Firat Deveci Petrica Barbieru if i use buck, duty will be very very small.

Like · Reply · 3w



Petrica Barbieru Yes, indeed. It's strange why they use 20-30V battery stack when need to feed an inverter for motor pumps. Maybe in 10-12 battery stage can use buck and increase overall efficiency by reducing cable / input inverter currents.

Like · Reply · 3w



Firat Deveci Petrica Barbieru They generally use PV directly connected to MPPT motor driver. So they are using 600-800Vdc. They are using batteries because of they run TV or something else at night. Batteries are not for motors. This is my idea, maybe customer uses it to completely different area.

Like · Reply · 3w · Edited



Petrica Barbieru Pirrat Deveci a... ok. In this case I think will be much better to add isolation even they don't requested... as topology, I'll try LLC with high gain range (1-5) below fr.

Like · Reply · 3w

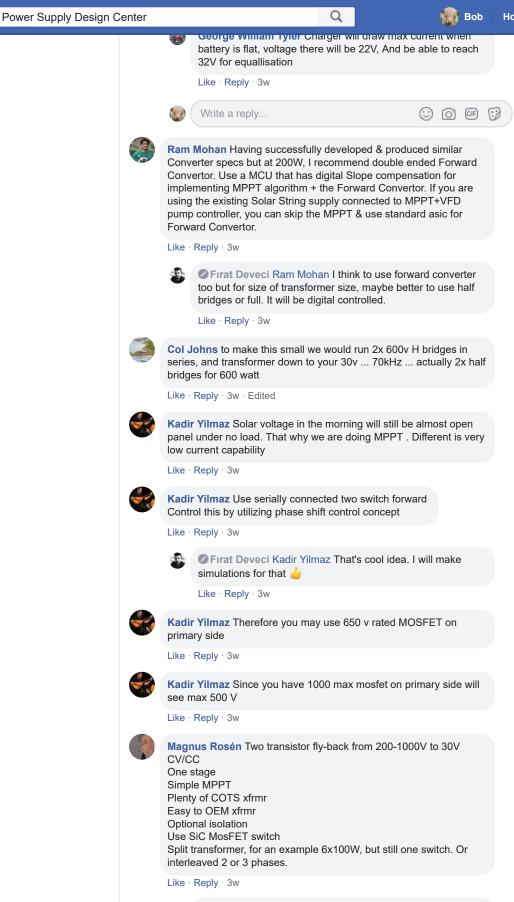


Fırat Deveci Petrica Barbieru I will use transformer. If switches fails, they will not damage batteries. But for LLC input range is very wide I think, I have to calculate.

Like · Reply · 3w · Edited



Petrica Barbieru Yes, it's very wide input range but may be covered by small Lm/Lr ratio. Need Lr to be separate... can't be leakage only, being high value (at least for "normal" sw freq).





Firat Deveci Magnus Rosén What about reflected voltage level? 1200V fet will be not enough.

have to observe some limitations of turns ratio and duty cycle range. And it's slightly moore complex gate drive for top switch. Vds 1200V may be sufficient. If solar array overvoltage (transient/surge/etc) are limited to 1000V+200V. Your original idea with front buck stage PPT control from 1000-200V to 200V followed by f/b, fwd, llc, h/b or psfb stage is also good. As W Tyler suggests.

The problem is when planning breakfast, there is too many ways too cook an egg 🗨 🥥 🧼

And this forum has many master chefs with their favourite recipe haha.

BTW - doing this equipment without proper insulation between input solar array and output accessible couplers is noot feeling good. Does it?

Like · Reply · 3w · Edited



Fırat Deveci Magnus Rosén Oh sorry i didnt see 2-T flyback. You are absolutely right 🍐

Like · Reply · 3w



Magnus Rosén If the 2T is perfect, tDelay, tR/tF the switch transistor may have Vds rating (Vfb+Vin)/2. But in practice hard to achieve. Drawback is EMC when isolation transformer conversion from high Vin. That's why step down to 200V may be overall better, even if 2 conversion stages.

Like · Reply · 3w



Firat Deveci Magnus Rosén What do you think about boost the voltage and then using half/full bridges. I want to make it boost because for 600W output power, input switches rms current will be 1-1.5A. In this case i can use IGBT at 1200V and they are very cheap.

Like · Reply · 3w



Write a reply...











Yuri de Klerk Many possibilities off course, but which one's better? I've got one:

Buck converter in the negative solar path to 200V. So no high-side driver required. Second stage can be any topology easy to make, even with LLC IC with integrated high side driver.

Maybe single stage can reach higher efficiency but 1000V high side driver is harder to make and wide range input with galvanic isolation will bite efficiency goal.

So now I just see I actually second George William Tyler

Like · Reply · 3w · Edited



Col Johns If the input is never going over 1kV then an LLC half bridge with 1200V fets will work just fine too say 50k - 100kHz to keep the Tx simpler ...

Like · Reply · 3w



David Seal Early-load "generation stall" prevention under partial cell illumination is the main reason for MPPT, though it does also ensure that the peak efficiency is maintained while partial illumination climbs to full. This also means that to prevent over-loading the input side under start-up, the output power must be adjusted gradually upwards as well, by matching the exact output voltage and current available to charge the battery. So not only do you have to allow for a wide input range, you must also maintain a precise output control as well, based upon the input conditions.

Like · Reply · 3w



Col Johns For pwm or freq control - this is pretty easy - just adjust pwm ( or freq ) to arrive at max power in, this will automatically adjust Vo / Io, have to limit the power when Vmax ( or I max ) is reached on the batt - we did this in analog for a very high volume, low cost design ( no uP ).

Like · Reply · 3w · Edited

lengths, installation, regulatory and national electrical code issues. There is a reason there are so few, great PV charge controllers on the market. It's not for lack of trying. The road is paved with good

Like · Reply · 3w · Edited





Col Johns @ Brian Faley - assuming there is only one peak power point at a given time (there may be some sub peaks) if a controller arrives at the true peak quickly - then 80% of the issues are solved ...? correct ..?

Like · Reply · 3w



Brian Faley Depends on how big the sweep is. I've seen tons of roof top systems with two large peaks get confused several times a day from sharp line shadows from plumbing pipes, overhead wires, or partial shade from roof dormers, or tree leaves. Very few roof tops don't experience some issues. Some happen suddenly, others gradually. How much power can you afford to leave off the table? How critical is the load? Sweep. Unless you're totally full sun all day, it's going to happen, until the sun starts to set and shading begins. (Or rises and stays off the real peak all day!)

Like · Reply · 3w · Edited



Col Johns Chaos theory and analog design ... ! Step one create a chaotic system at the PPPoint... Partial shading is a real power killer though ...

Like · Reply · 3w · Edited



Bob Gudgel Typically, the higher input voltage of 1000 VDC or 1500 VDC are going to be commercial solar farms and they will typically not have any shading. Solar/PV on homes, at least here in the US, are typically not higher than 600V open circuit. Until recently, those 600 Voc (more like 550 Voc) have not had batteries so much (in the US) Now, self consumption is starting to happen in the US so batteries will be more and more common.

Did you know that with the Tesla Power Wall system that they will not run for very long without an internet connection? So much for using them for off-grid systems

Like · Reply · 3w · Edited



Brian Faley Col Johns Partial shading is the reason SolarEdge and Enphase dominate residential grid tied solar systems. Module Level Power Electronics (MLPE) at the solar panel is the sure way to avoid the loss of power from more than just the shaded panels.

Like · Reply · 3w



Bob Gudgel Module level MPPT doesn't work quite as well as a chain saw though at reducing shading from trees 😃

Like · Reply · 3w

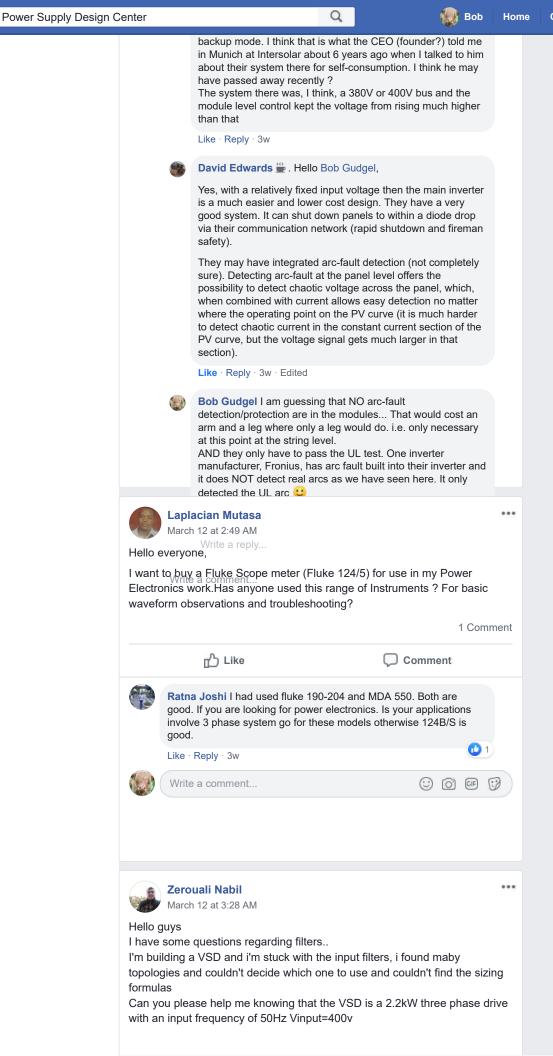


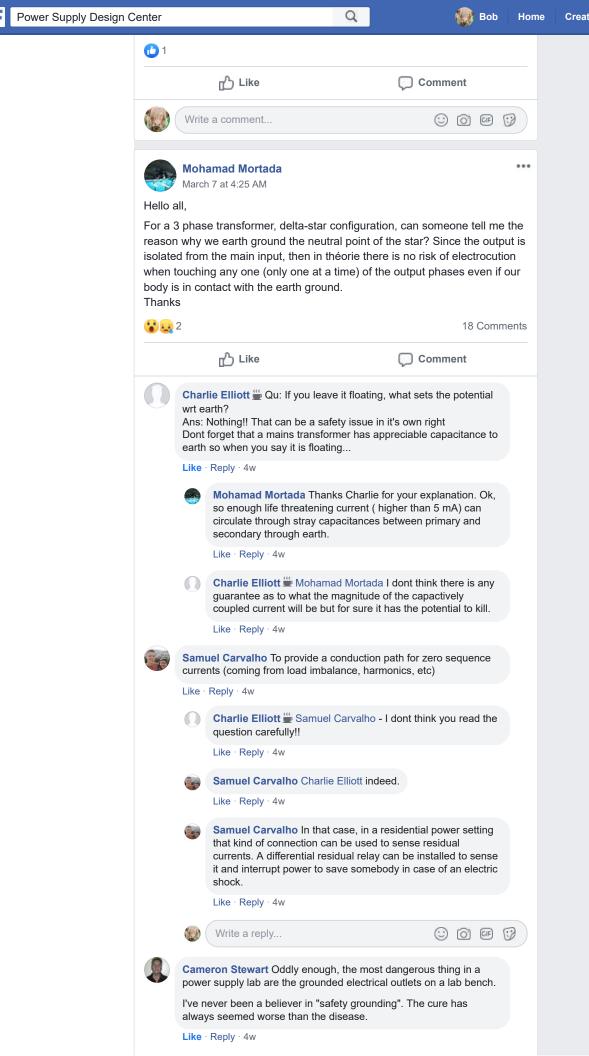
Brian Faley MLPE is quite good at preventing one or a few modules from shutting down the whole array. But like Bob Gudgel observed, sometimes you have to cut the trees back.

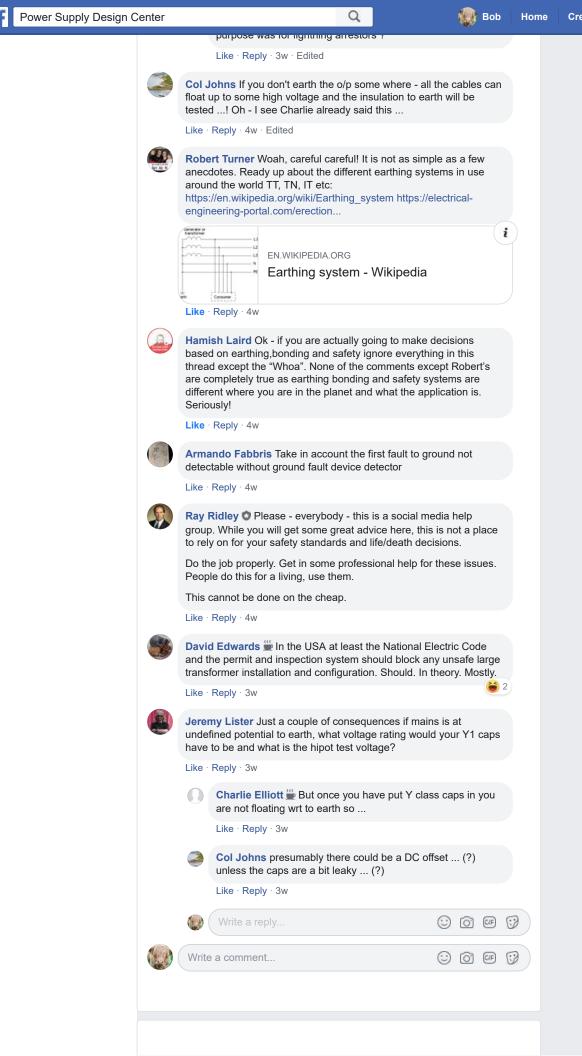
Like · Reply · 3w

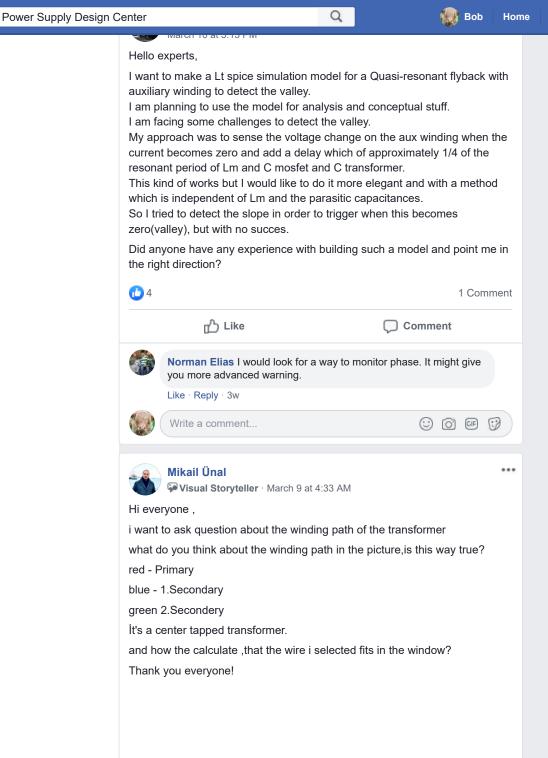


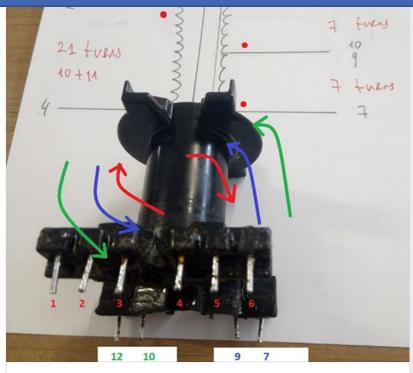
Bob Gudgel Yes, MLPE can help for partial shading BUT if the WHOLE module is shaded, then it doesn't do any better than the bypass diode(s) built into the module(s)











Q

30 Comments

i

i

Like

Comment



**Bùi Văn Cương** Last week, I had the same question, and I suggest you watch this video.

Like · Reply · 3w



**Bùi Văn Cương** https://www.youtube.com/watch? v=LuZh1QnegC4



YOUTUBE.COM

#209: Basics of Phase Dots on Transformer Windings

Like · Reply · 3w



**Bùi Văn Cương** https://www.youtube.com/watch? v=otzjJ9ZciW0



YOUTUBE.COM

Dot convention 2

Like · Reply · 3w



Andrew Ferencz Simple for winding on a bobbin, I use the dot side for either clockwise or counterclockwise. Even if you have two windings with a common connection (center tapped), each winding starts and ends. And I try to wind so the wires don't cross at the pins.

Like · Reply · 3w



Ram Mohan Quite simple. Rotate the Bobbin clock wise & follow the instruction

- 1. Wind 21Turns clock wise. Start Pin 2 finish Pin 4.
- 2. Wind 7 turns.clock wise Start Pin 7 finish Pin 9 & 10.
- 3. Wind 7 Turns clock wise. Start Pin 9 & 10 finish Pin 12 Thats it!!. For calculating the Build, you need to calculate the Ap (Area Product) required for the respective Power levels, Output Current, Frequency, insulation, Topology. Then chose the nearest Core & bobbin that fits

Like · Reply · 3w · Edited

















Like · Reply · 3w

Ram Mohan Mikail Ünal Only if you have to wind the 2nd half center tap winding on top of 1st half center tap.

Like · Reply · 3w

Mikail Ünal Ram Mohan can i send a video to you if i do it right or not?

Like · Reply · 3w

Ram Mohan You can send it here i guess if the Admins permit so that others can comment or learn!

Like · Reply · 3w

Mikail Ünal Ah oke thats better!

Like · Reply · 3w

Mikail Ünal P This is the winding video, Note: i have put isolation between s1&s2 I dont know that this a true winding technique is, Im waiting you're comment guys thank you again.



Like · Reply · 3w

Ray Ridley that man could use a winding machine in the lab 🤓

happy to see you making your own.

Like · Reply · 3w

Ray Ridley what is the winding order that you are using? cant really tell from the choppy video.

Like · Reply · 3w

Mikail Ünal Ahah yes sir that's true my opinion is that we need to start from the basic to become a master

The order is 10+10 primary (to minimaze the leakage)

And the Secondary is 7+7 (center taped)

Like · Reply · 3w

Ray Ridley OK, how about more details - you have two primary layers, and two secondary layers. that is 4 windings.

What is the order in which you put them on the bobbin?

Also we need to know your topology.





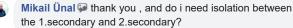




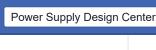


























10-12 2.secondary

I'm going use this transformer in a phaseshifted full bridge converter wich will work in 100-240vac

My irms current on the primary side is 12A And on the secondary side is it 18A

I have set the current density almost to 4a/mm2

For the primary winding 18x0.45mm wich has 3mm2 area Ans for the secondary 28x0.45mm wich has 4.5mm2 area

Like · Reply · 3w



Mikail Ünal Also i have calculated the max wire diameter for the transformer that will work in 100kHz and how many power the transformer will carry , my output power is almost 750watts and the transformer can carry more than 1400watts

Output power of the converter 30vdc 25A

Like · Reply · 3w · Edited



Ram Mohan Is that a PQ36/30 Bobbin?

Like · Reply · 3w



Ray Ridley OK still need more. How do you wind the two layers of primary?

Like · Reply · 3w



Ray Ridley © Can we see a primary impedance sweep, open and short circuit?

Like · Reply · 3w



Ray Ridley That is three short circuit sweeps, each secondary at a time, then both together.

Like · Reply · 3w



Mikail Ünal i have take photos maybe it should be better In this picture i have wind the first but half primary with 10



Like · Reply · 3w



Mikail Ünal and in this picture i have wind the 1. secondary i was becarefully with every layer so therefore put isolation everywhere.



Like · Reply · 3w · Edited



Like · Reply · 3w



Mikail Ünal and the last look of the transformer is in the picture what i did is the winding of the other half primary and also the center

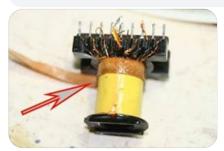
Q



Like · Reply · 3w · Edited



Janaki Ram Gopal Pagolu You have to provide creepage distance between windings, i.e. between primary and secondary to prevent input a.c. supply to appear at the output (by insulation breakdown). This is done by providing margins at top and bottom of the winding. Creepage distance depends on the insulation on wire and tape you use.



Like · Reply · 3w · Edited



Mikail Ünal A Janaki Ram Gopal Pagolu ah thank you for giving this advise i will isolate it much beter this is a prototype , but what about the winding path and the center tap is it right?

Like · Reply · 3w



Janaki Ram Gopal Pagolu Mikail Ünal I always kind of cheat in this step, I wind the transformer in which ever way (CW or CCW) possible and in the end I apply sine voltage from signal generator, compare input output waveform, and swap the terminals if requirement is not met

Like · Reply · 3w · Edited



Write a reply...





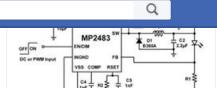






Markus F.L. for symetrie is better the sek winding Bifilar...





Like · Reply · 4w

David Edwards "Is this the first time you have applied power to this PCB assembly? If so, please check all the IC pin numbers to the PCB. Perhaps there is a layout mistake. Perhaps SW is shorted to ground (D1 is backwards?).

Like · Reply · 4w

David Isaias Jaimes Reyes David Edwards yes, is the first time

Like · Reply · 4w

David Wigton David Isaias Jaimes Reyes Next time currnet limit the bench supply.

Like · Reply · 4w

David Isaias Jaimes Reyes David Wigton is the current?

Like · Reply · 4w

David Isaias Jaimes Reyes David Wigton



Like · Reply · 4w

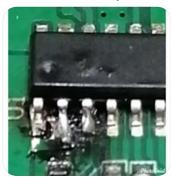
David Isaias Jaimes Reyes It is the power supply bench

Like · Reply · 4w

David Wigton David Isaias Jaimes Reyes You can limit the current on the supply where it says current. Set it before attaching to your supply. It's hard to tell in the PCB picture what burned, can you get a close up of the damaged area?

Like · Reply · 4w

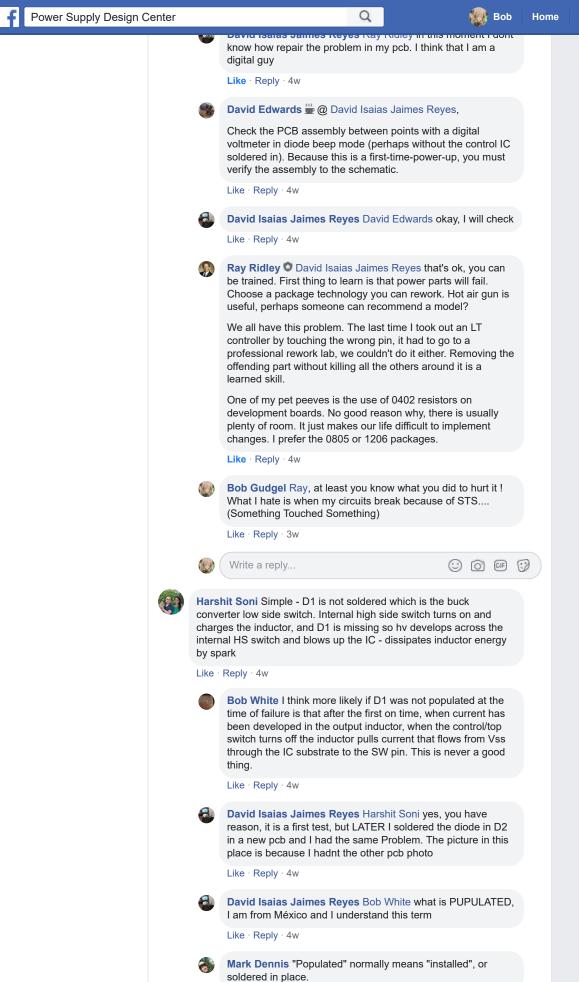
David Isaias Jaimes Reyes

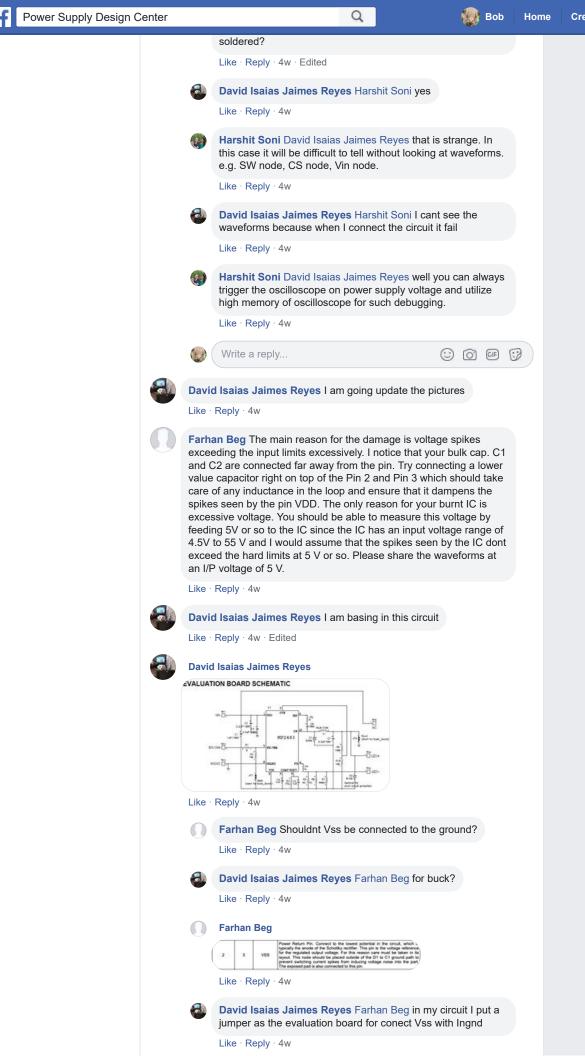


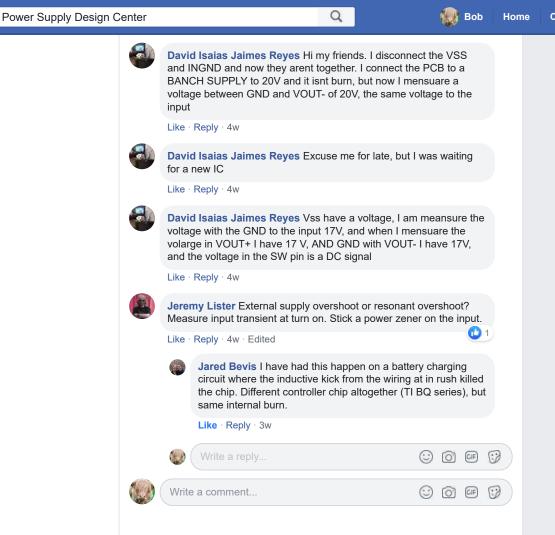
Like · Reply · 4w

David Isaias Jaimes Reyes









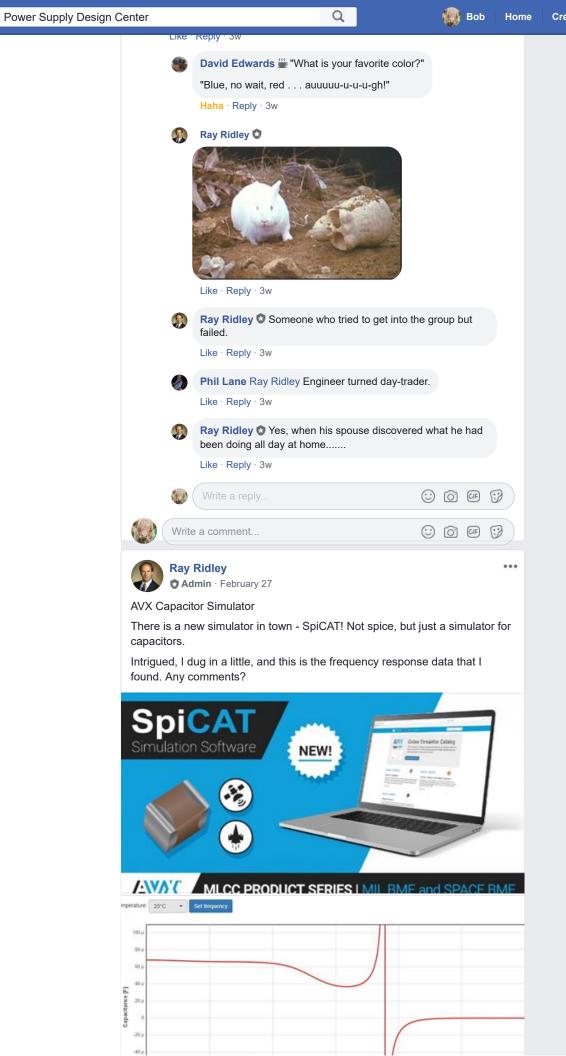


**New Group Members** 

Please make sure that you let new potential members know that they MUST answer the questions to be a part of this group.

This has become a legal requirement in the US now, we cannot accept them if they don't answer. It's not just us - you will see similar questions being asked if you try to download free software and other design information from the big companies.







**Kevin Azul** 



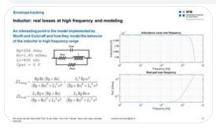
but i do like their circuit models, very sophisticated and usable.

Now, if only we can get the magnetics manufacturers to put out a circuit model too. So far they are resisting that strongly. I will keep banging this drum because it is getting ridiculous at this point in our industry.

Like · Reply · 5w



Riccardo Tinivella the new spice models of coilcraft and wurth have Rac (only proximity) inside, I check also them by measurements and they are also quite ok (till 5MHz) let's say



Like · Reply · 5w · Edited



**Darrell Hambley** Gotta be suspicious of the person who made that pic. That resistor value would only be accurate at one unique frequency and peak flux level.

Like · Reply · 5w



Ray Ridley That model won't work for proximity. Its a fixed series resistor, and the parallel resistor is for some representation of core loss. About as crude a model as you can get.

Straight out of the texts of 1898.

Like · Reply · 5w



Ray Ridley Magnetics - dragged kicking and screaming into the 20th century.

Better late than never.

Like · Reply · 5w



Claude Abraham I've used it & really like it. It provides useful data.

Like · Reply · 5w



Thomas Mathews I still contend that, because it shows negative, as well as zero capacitance, that this graph is bogus. The Y-axis is probably supposed to be j\*Ohms not uF. OK, so negative capacitance is not totally impossible but I see no gyrator in this circuit so color me skeptical.

Like · Reply · 5w · Edited



Ray Ridley You are quite right. They have a lot of good data and models, but this particular graph is bogus. AVX have a history of this, plotting capacitance vs frequency and having it drop to zero at the resonant point.

they don't do it for their MLC parts, just the tantalum (based on my quick look at their program.)

Good job though for the circuit models. If the cap makers can do it, its time for the magnetics vendors to up their game. We have shown them how to do it, but they don't want to go their yet.

Like · Reply · 5w



**Col Johns** I just can't get over the fact that they are plotting Z not C - yet put C on the axis - where is the real understanding? C does not go to some ultra high value ...

asked it to extract an RC model (no L) then it made the equivalent cap go to zero at the resonance. All their MLC parts were plotted this way.

Seems they have learned not to do this any more, but maybe some legacy measurements remain.

Like · Reply · 5w



Ray Ridley Doesn't make sense for a cap vendor too say their part goes to zero at some frequency. People get easily confused and won't buy it.

Like · Reply · 5w



**Col Johns** This seems like sales people with no engineering degree - just plot Xc vs freq and put a big red arrow at SRF with an asterix and note at/on the graph - above SRF plot XL ... this is very instructive for high quality electrolytics ...

Like · Reply · 5w



Claude Abraham Actually, their interpretation makes sense, but is sloppy. For a series L-C network, impedance can drop to near zero, at resonance. This zero impedance is equivalent to a zero inductance value, or infinite capacitance value.

Likewise, a parallel L-C has a very large impedance at resonance. This can be modeled as an infinite inductance, or a sero capacitance. A capacitor of 0 farad has infinite impedance at any finite frequency.

I agree with the posters above, that their terminology is sloppy.

Like · Reply · 4w



Stephen Ziel I've been using these models for as long as they've been around. I don't really look at the curves other than impedance. I think at some point it all boils down to the equivalent impedance of the capacitor across frequency. Other manufacturers are starting to provide their own capacitor models. Murata has a triple resonance near the minimum impedance for their X7R caps, and their ladder network simulates that.

Like · Reply · 3w





David Edwards . Hello Ray Ridley,

This graph is of capacitance (which has no phase). At resonance it switches to inductive (which is plotted as a negative capacitance). The magnitude just switches polarity, but never really goes through zero. A better plotting program would not plot the vertical line at the polarity change..

Like · Reply · 3w



**Colin Tuck** Surely the graph is of Ztotal not capacitance ... even then it is wrong ...

Like · Reply · 3w · Edited

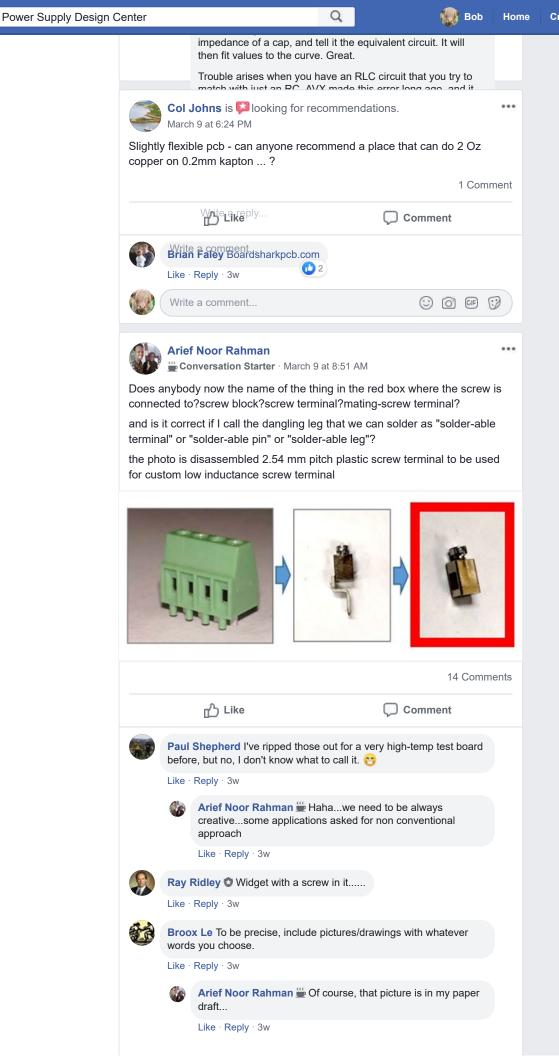


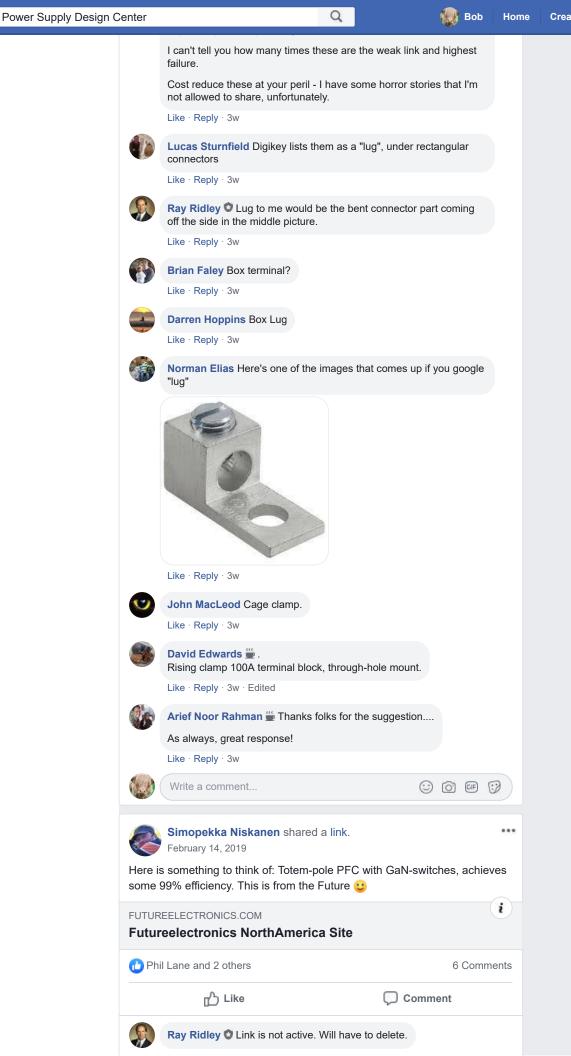
David Edwards w Look at the y-axis label.

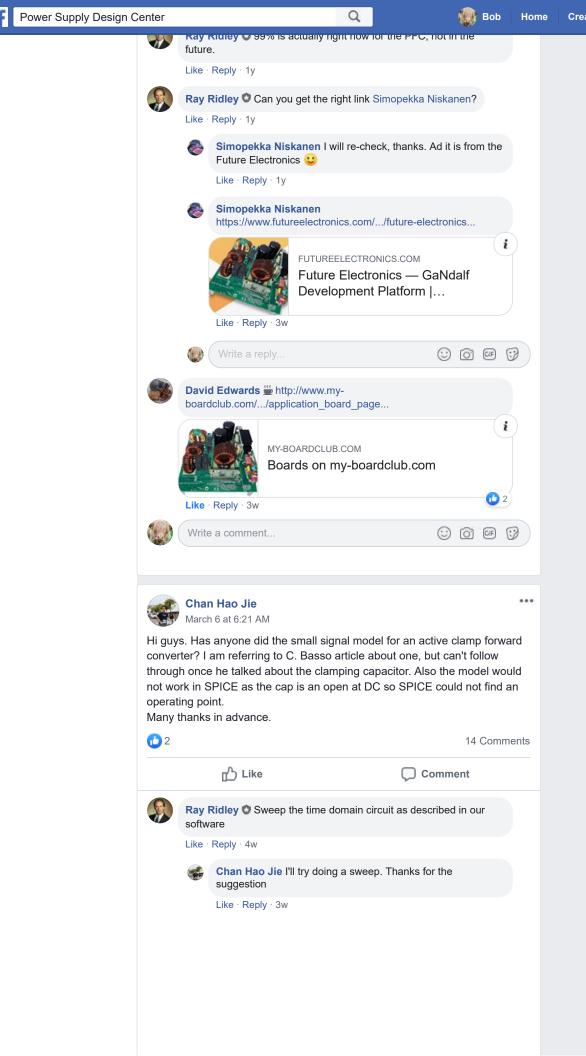
Like · Reply · 3w



**Colin Tuck** I would but it's wrong - the C doesn't and can't go from + infinity to zero to - infinity over a short freq span ... and then to zero at VHF ... tis quite the piece of crap graph ...







Home

- 1. Correct active (ground), passive (clamp branch) and common (magnetic) terminals
- 2. Correct voltages mean values (both active to passive and common to passive terminals). I used it. Further the clamping cap is linear per se and can be placed as it is.

I'm writing a tribute chapter for a SMPS book concerning his elegant approach

Like · Reply · 4w · Edited



Steve Den Voltage Mode or Current Mode?

Like · Reply · 4w



Nicola Rosano Steve Den VM, the model is available. Or you can proceed, as I did, from scratch to crosschek with available

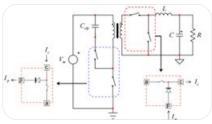
Once you enclose the 'non linear part', mos + clamp diode couple you can apply Vorperian approach.

- 1. Identify the three terminal cell (mentioned before)
- 2. Average active, passive, and common current. Repeat for two voltages (active2passive, passive2common, active2common with Kirchhoff voltage law). You have the large signal model.
- 3. Partial derivative to get small signal. Trust me, if you grasped Vorperian approach, it is more hard to explain then try

Like · Reply · 4w · Edited



#### Nicola Rosano



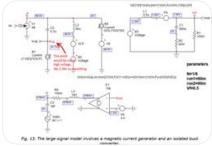
Like · Reply · 4w



Chan Hao Jie Nicola Rosano Hi Nicola. I tried following his approach, and I had a roadblock.

The image is from "The Small-Signal Model Of An Active-Clamp Forward Converter (Part 2)"

Vclp node is showing high voltage in LTSpice, which makes sense, because it's a cap in series with a current source. I am not sure how to approach this. Looks like his ISpice is working



Like · Reply · 3w



Write a reply...







i



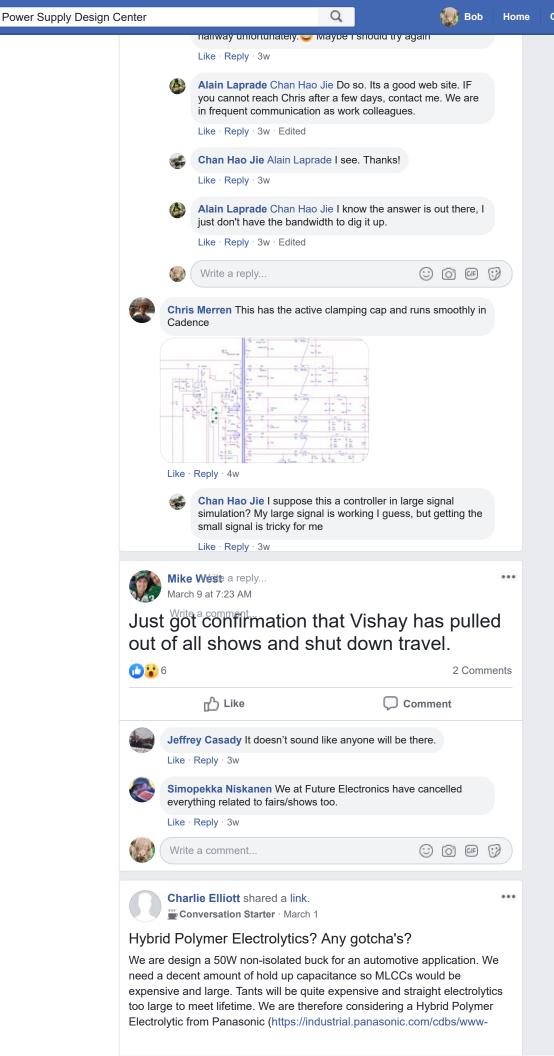


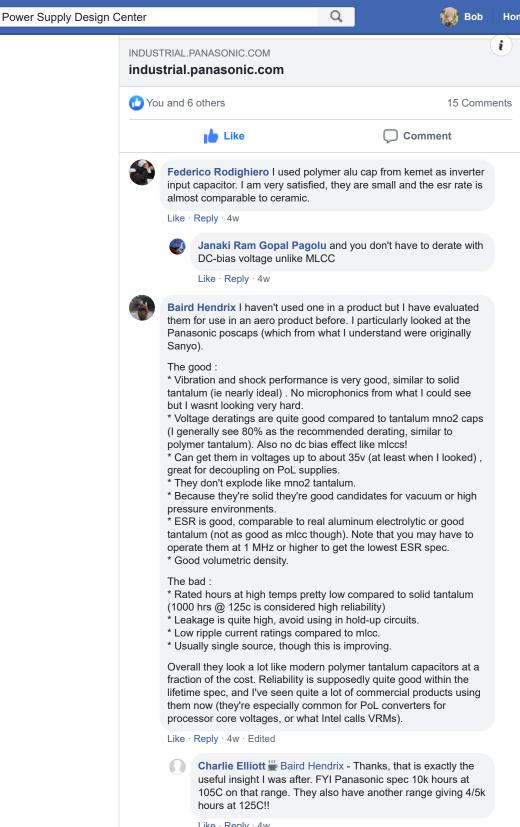
Alain Laprade You might want to consider dropping a note at Christophe's web site asking for guidance. https://cbasso.pagesperso-orange.fr/



CBASSO.PAGESPERSO-ORANGE.FR

Welcome





Like · Reply · 4w

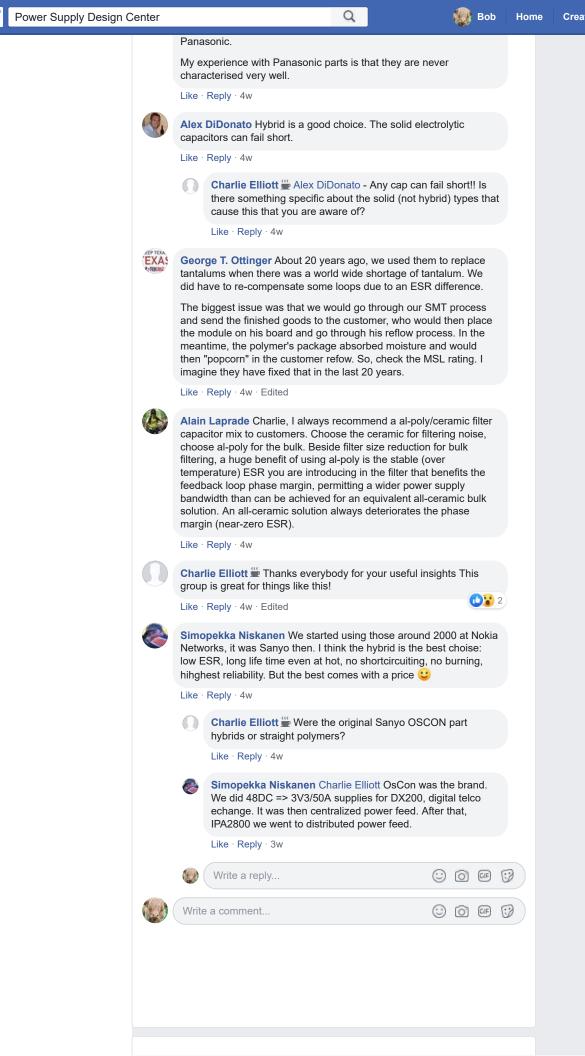


Anil Adapa They are good, we have been using the same series (from Panasonic) for the past 5 years. Application is a 300-400 kHz half-bridge inverters with 24V dc and power levels for 10-25 W.

Like · Reply · 4w



Lucas Sturnfield They are quite good. Nice and space dense. The above commenters put in the bads (single source, price, lower ripple current, etc). I would offer an experience that this series really doesn't like to be overvoltaged and they will pop aggressively (not unique in caps of course, but still an aggressive failure mode)



Q

TI's New Design Software - RidleyWorks 0.001

It was mentioned in a thread somewhere here, but I pulled this out. TI have realized what we have known for 30 years - Excel is the perfect platform for design. Presentation of data is unsurpassed, and it is a great multivariable environment.

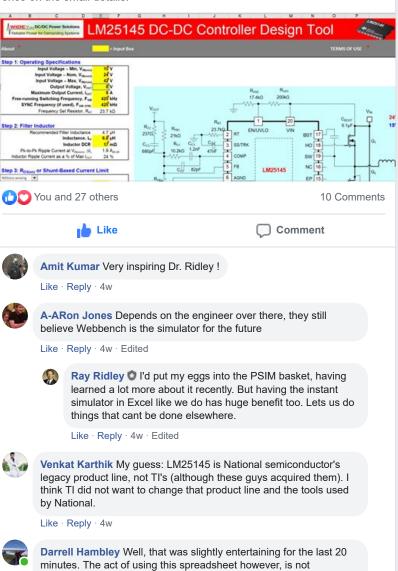
Easy for all to follow and understand since they know Excel, we all have to use it.

Now, their product is where we were in 1991. It designs the controller compensation. They have a lot still to learn about how to make Excel work for you. Data presentation is still spreadsheet-think, cluttered, and too much data at once. We started there too.

I don't think they will ever take our next step - running the large-signal simulation inside the Excel spreadsheet. We do it more efficiently that anyone can simulate a circuit. We could teach them how to do it, but they are not going to ask, we know that.

Incorporation of proximity loss and full magnetics design? Maybe in another 30 years or so.

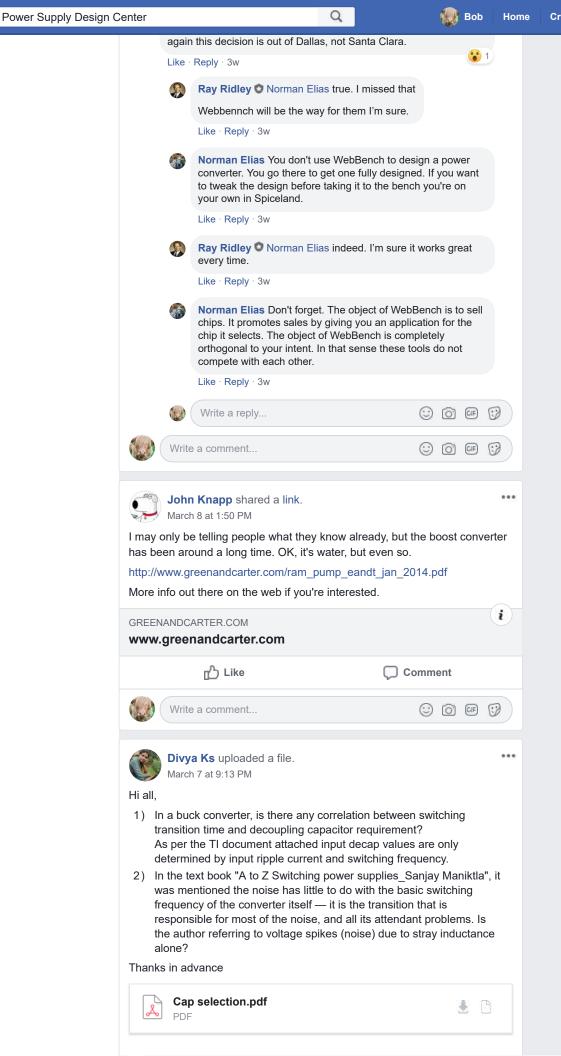
Regardless, congrats to TI on arriving at the right playing field. Better late than never! We can even see some cute things they have done that we may adopt in RidleyWorks. Nice to have another programmer to lead the way for once on the small details.

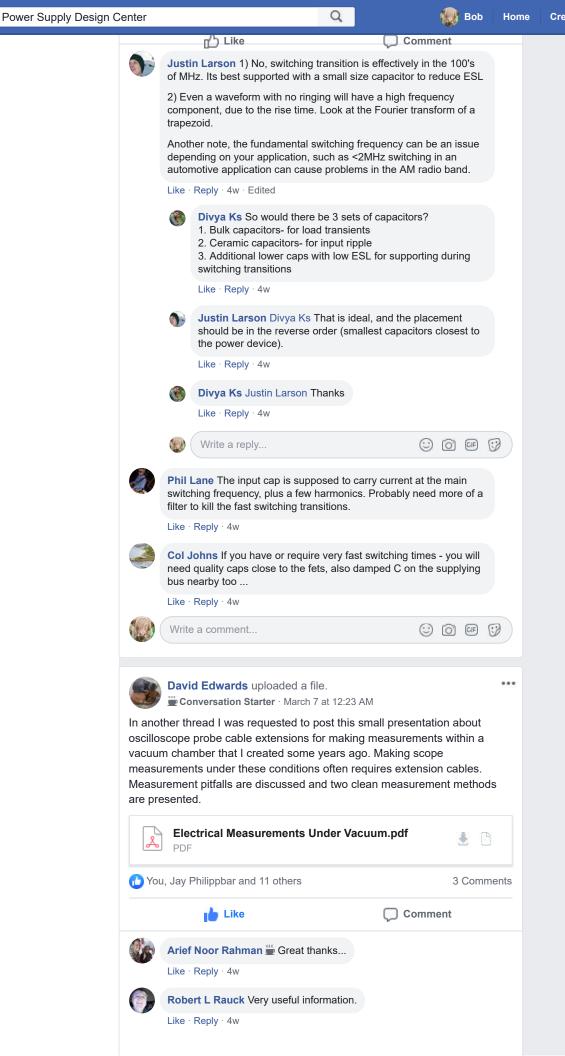


"designing"; rather it is "hacking" or "shot gunning" quickly. I believe none of these "design it for you" programs are a substitute

for an understanding of 'Control Theory 101'.

Like · Reply · 4w · Edited





32 Comments

Comment

**6** 5

Like

i





pretty safe, no ground lead (and common-mode noise issues). You are basically making your own probe with resistors on the board. You need to consider the voltage rating of the resistor. 1206 500V rated resistors are pretty inexpensive.

Like · Reply · 4w · Edited



Arief Noor Rahman I know I am like trying to make my own probe, but the difference is location of resistive divider that is close to the scope BNC, instead of close to probe tip as normal probe

I got the idea by watching EEVblog video https://www.youtube.com/watch?v=qpwkiJC5hfU

my problem with that pcb to probe adapter is...it is big, and my space for measurement is very crowded with 3 test points next to each other...



YOUTUBE.COM

EEVblog #1266 - PSU Probing Screw Up!

Like · Reply · Edited



Andrew Ferencz A scope is 'unbalanced' .. and any common-mode current will flow in the ground lead (low impedance) rather than the tip. Thus all CM current flows in the ground and you get a V=Ldi/dt .. which isn't 'real' if you are interested in the differential signal. I don't think an SMA connector is smaller than a 5mm probe tip ..

Like · Reply · 4w



Arief Noor Rahman Andrew Ferencz the measurement point itself is referred to ground as well...

the problem is although the probe tip is small, but, the probe body is considerably larger...and if I use pcb to probe adapter it will be much larger than SMA connector...if use as the picture above, the probe can fall easily

Like · Reply · 4w



Andrew Ferencz you can route your measurement point to a better location, the key is a good ground plane for the scope, not a skinny trace.

Like · Reply · 4w



Arief Noor Rahman W Andrew Ferencz could you please elaborate on "good ground plane"?

Like · Reply · 4w



Write a reply...













Arief Noor Rahman # I just noticed that 50ohm coax has ~1pF/cm capacitance...so, perhaps this approach may increase the capacitive loading compared to 10x probe...

Like · Reply · 4w



Alex Berestov Think before you do. Nobody prohibits you from competing with the scope industry.

Like · Reply · 4w



Dave Lafferty I have used that before. Small sma or other small rf connection on the PCB to measure ripple.

Like · Reply · 4w



Arief Noor Rahman # May I know your freq of interest and the signal amplitude?



Like · Reply · 4w



Arief Noor Rahman # I did that already...but I am looking to make it more physically stable...now is okay but i want to improve it

Like · Reply · 4w



Thomas Mathews A 10X probe simply has a 9 megaOhm resistor in parallel with a variable capacitor. The vari-cap has range that includes a value that is ten times lower than the input capacitance of the scope and coax combined. You could build the 9 MegaOhm and varicap (maybe 0.3pF to 3.0pF type) onto your PC board then connect via coax to your 1M-Ohm scope with an SMB or SMA. To adjust the compensation capacitor, you'll have to figure out how to get a square wave "calibration" signal to the input side of this structure. Make sure the 9 megaOhm resistor you use is up to the 400V signal as most chip resistors are only good for 200V max. If you use chip resistors consider several in series that add up to 9 megaOhm.

Like · Reply · 4w · Edited



Arief Noor Rahman Thanks Thomas Mathews

Like · Reply · 4w



Kristian Kruse An oscilloscope cable is not a regular coax. As far as I know, it is a lossy line, which helps to minimize standing waves and ringing.

If I remember correct then Dave from EEVBlog has a video about the subject.

Like · Reply · 4w



Thomas Mathews Yes, that is probably true but this will work to some bandwidth. If you want flat response to many hundreds of MHz then, as you point out, finer details may need attention....

Like · Reply · 4w



### Kristian Kruse Thomas

I might be wrong. But isn't the high bandwidth is exactly what you want, when you want to measure the high dV/dt and ringing of a GaN HEMT switching?

Like · Reply · 4w



Arief Noor Rahman Fes...you are right Kristian

Kruse...scope probe has 300ohm resistance...they must do it because they want to have very long cable and flat freq response

I read somewhere that if cable is shorter...the signal reflection will be less of an issue, thus no need for an lossy transmission line

Thats why I am considering to use only 10~15cm cable

Like · Reply · 4w



## Kristian Kruse Arief

How high bandwidth are you aiming for? And how will you verify that the bandwidth and linearity is correct?

Like · Reply · 4w

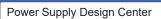


#### Arief Noor Rahman W Kristian Kruse

I dont have any number to shoot for ...

I also have no clue on how to verify since i need 1Mohm probe input impedance while most VNA or spectrum analyzer has 50ohm input impedance

I guess, just compare with our passive 500MHz tek probe, if looked similar then call it good enough









i











Daniel Ruiz I've gotten good results embedding the voltage divider to create a 10x and 100x probes in the PCB, run it through a high-speed amplifier, then out via SMA into the scope in 50ohm impedance mode. Use the vari-cap as mentioned above to compensate you "probe." Alternatively you can use discrete caps to create a capacitor divider in parallel with your voltage divider. You are trying to keep capacitive mismatch between the two resistors from distorting your measurement.

A couple of tricks I use to avoid having to hold the probe with my hand, which you may not have the luxury to include on your board (but others may find useful):

1. add a pair of holes on the PCB with the right spacing to directly insert the probe tip and ground clip (see Figure 5 in this doc: http://www.ti.com/lit/ug/snvu551/snvu551.pdf).

2. add a fuse-holder clip with the right inside diameter to fit the barrel of your scope probe placed in such a way that you can slide in the probe and contact the point of interest witht he probe tip, which keeping a solid and snug ground connection to ground.

 $Like \cdot Reply \cdot 4w \cdot Edited$ 

Write a reply..



**Thomas Mathews** All analog/RF labs should have one of these: https://www.mathews-engineering.com/.../High\_Impedance...



MATHEWS-ENGINEERING.COM

# High Impedance Buffer Amplifier

Like · Reply · 4w



David Seal Nice product, well thought out, reasonable cost.

Like · Reply · 4w



Arief Noor Rahman We Nice touch

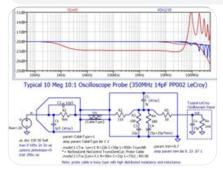
Like · Reply · 4w



David Edwards ∰ Probe cables are very application specific and of unique construction:

- \* Very low per-foot capacitance for small diameter cable (~16 pF/ft)
- \* Special spiral wound high resistance center conductor (226 ohms)
- \* Provides controlled high per-foot resistance (~75 ohm/ft)
- \* Also provides distributed peaking inductance (~1µH total)

Attached is a schematic and simulation plot of a typical 10x oscilloscope probe. The plot shows the effect of changing probe cable to 50 ohm RG-58.



Like · Reply · 4w



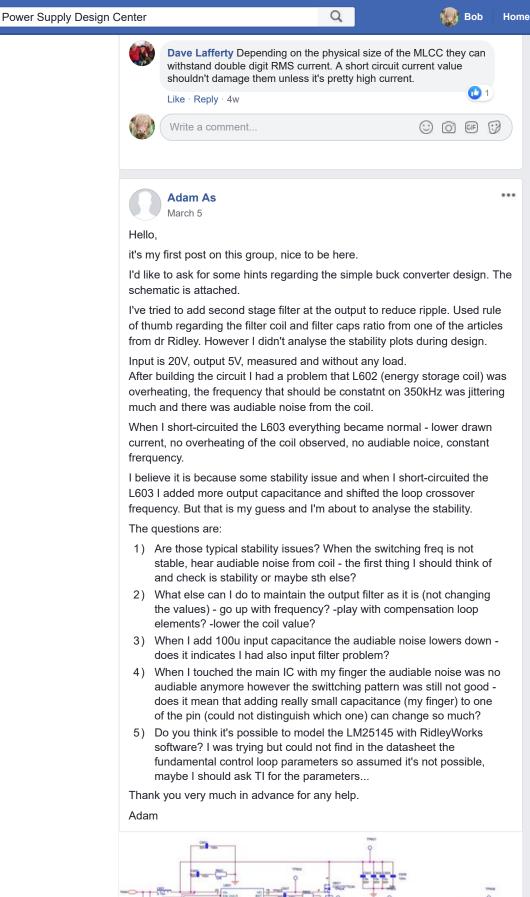
David Edwards The red trace is with the wrong probe cable (RG-58 50 ohm). The matching networks are for the special probe cable and would need to be adjusted to work with the RG-58 cable. However, the real problem is at high frequencies.

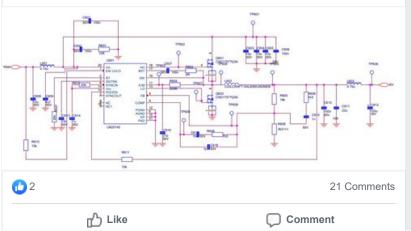
Like · Reply · 4w



Question:

If short circuit happens in the circuit through MLCC ( the ceramic caps ) which supposedly supply the short circuit current Is it reliable to keep using that cap after the circuit is fixed?





i

issues. (1) PCB noise/EMI (hint given by your 'finger test' on the main IC), potential stability issue. Do you have the capability of measuring the feedback loop (modulator plot, op amp response, open loop in closed loop form)? I think Ray's software would also be helpful given datasheet parameters (Ray can better comment on that for a 2 stage output filter). TI has a model on their web site. Did you attempt to use it?

Q

Like · Reply · 4w



## Casper Hjort Wilson Try to:

- Increase C609 (input cap)
- Switch output caps C611 and C612. I believe C. Basso has an app note from OnSemi about addition of L-C post-filter impedance on a Flyback. As I remember, the larger C (in uF) should be closest to the Buck choke.

Like · Reply · 4w



Adam As Thanks.

Like · Reply · 4w



Adam As Regarding the caps order please see: http://www.ridleyengineering.com/.../86-052-designing-a.... Recomendation for doing it the way I did.



RIDLEYENGINEERING.COM

Ridley Engineering | - [052] Designing a Two-Stage Output...

Like · Reply · 4w



Casper Hjort Wilson Also, consider a RC snubber across lower FET. Check ringing on oscilloscope.

Like · Reply · 4w



Michael Thomason The output filter is not dampened. Also the input filter has the dampening cap smaller than the input bulk. Can you capture and post input and output waveforms? Filter output imp vs converter input? Bode plot?

Like · Reply · 4w · Edited



Yuri de Klerk I wondered if the output cap is e-cap or not. For damping an e-cap with esr > 0.1 Ohm could be helpfull. About the input filter I agree with Michael Thomason: The dampening cap should be a larger value than input bulk.

Like · Reply · 4w



Adam As regarding input filter is it a rule of thumb to have biggest cap near the input (having the pi filter at input)? I checked Middelbrook criteria with this configuration and it was

Like · Reply · 4w



Christophe Poupart LM25145 is a voltage mode control. Contrary to current mode control, L602 can't be neglated and introduce one pole power frequencyresponse. So, with voltage mode control, it's very difficult to defined a good stability corrector. With a second LC filter, your buck could be unstable.

Why Adding second LC filter?

To reduce ripple output voltage, you have to follow the datasheet to estimate the LC output filter and estimate the voltage loop corrector. Low esr capacitor could help you.

Without network analyser, Loadstep test will help you to evaluate stability margin.

Like · Reply · 4w



Adam As Hi, thanks. This article shows quite big advantage of using second LC filter, and remarks that it is not influencing the gain loop. However now I noticed that it could be only the truth with current-mode...

http://www.ridleyengineering.com/.../86-052-designing-a...



Ridley Engineering | - [052]
Designing a Two-Stage Output...

Like · Reply · 4w



Claude Abraham I am a freelance contractor now. If you need a pro to help you, I've designed nearly 100 power converters. No minimum hours. If you only need me for a few hours, that is fine. I can help you.

Like · Reply · 4w



Nikhil Joshi Check placement of loop compensation components ,see if it's ground and IC's ground is common and should have minimum track length possible.

Like · Reply · 4w



Jimbo Hissem Did you follow the datasheet application information? You need to find the correct output L and C to get the ripple you want, adding a second filter is unnecessary.

Like · Reply · 4w



Adam As I thaught that second filter solve the ripple problem and I do not need too much care about L and C values. I mean not much care - of course I checked this with Webench Designer from TI and was ok. But I could not simulate the second filter and just put large cap at output(so as there was no second inductor)

Like · Reply · 4w



**Jimbo Hissem** Adam As You need to design the L and C to meet your requirements, and then adjust the compensation accordingly. There is no reason to add second filter and it's only causing you problems.

Like · Reply · 4w



Frank Warnes You didn't move your feedback connection to after the second filter did you as this would really screw up your compensation

Like · Reply · 4w



Adam As this could be the clue... however I thought feedback connection point before filter does not influence the gain loop

Like · Reply · 4w



Christophe Poupart To help you, you can go on TI web site and use the Webench Designer (near technical documents) http://www.ti.com/product/LM25145

You will find schematic, layout and simulation tool. You could simulate Bode, startup...

Like · Reply · 4w



Like · Reply · 4w



Ray Ridley tis like RidleyWorks from 30 years ago, that is where we started too. Just a bode plot or two.

In two years we had waveforms added. Full simulations.

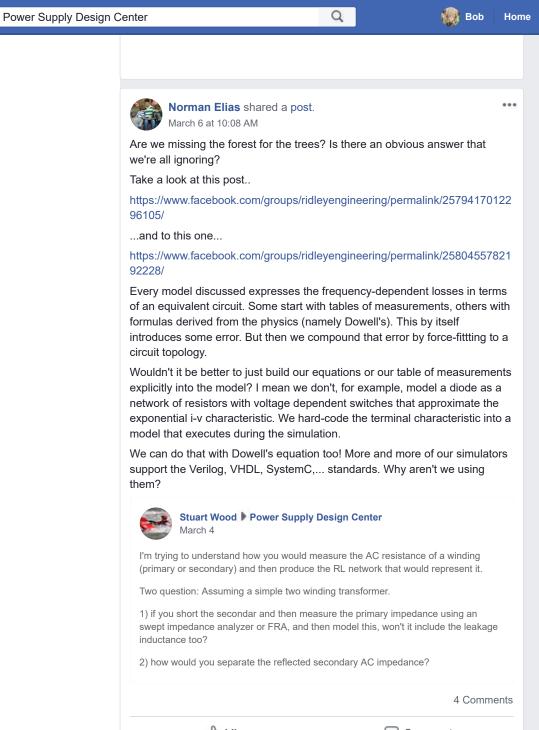
Glad to see TI catching up.

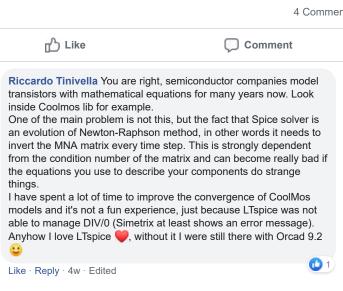
Like · Reply · 4w

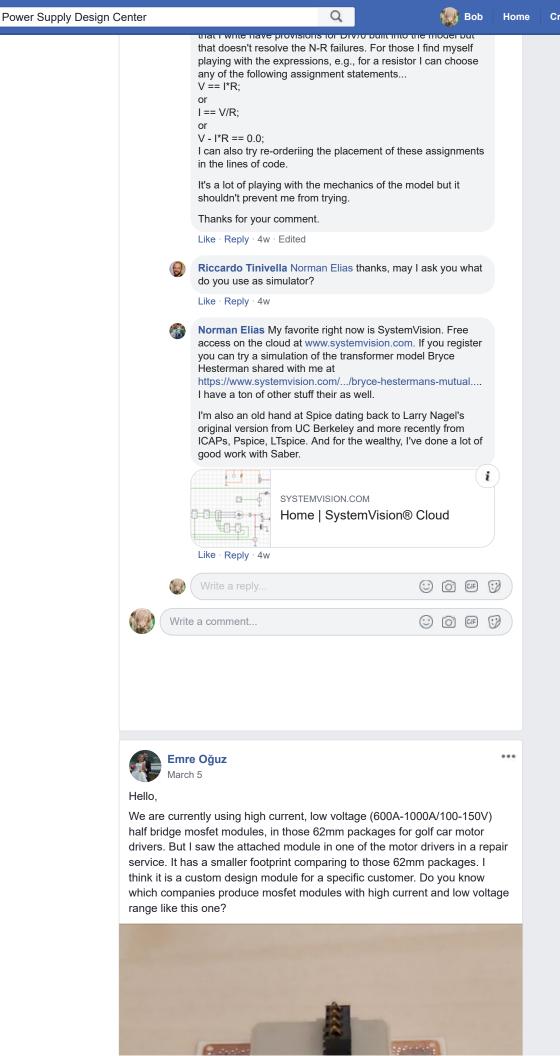


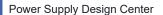
Ray Ridley Next thing, TI will be starting to sell magnetics - oh, wait, they just started doing that too!

It's an interesting world for engineers right now. Nothing is what you thought it was.









Home



Q



18 Comments







# Gà Tuấn Hust Phùng-Tuấn

Like · Reply · 4w



Gà Tuấn I think we are too backward, sirr

Like · Reply · 4w



Phùng-Tuấn Hust Gà Tuấn ừ công nhựn

Like · Reply · See Translation · 4w



Michele Bergo SME group

Like · Reply · 4w



Emre Oğuz Gà Tuấn It is not about being backward, it is about the quantity and economic potential. If we had a potential over 100K units every year, the MOSFET company would find us. Unfortunately, as a startup company, we have to work with standard components from trusted suppliers, because our demands are much lower.

Like · Reply · 4w



Write a reply...











i





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Like · Reply · 4w

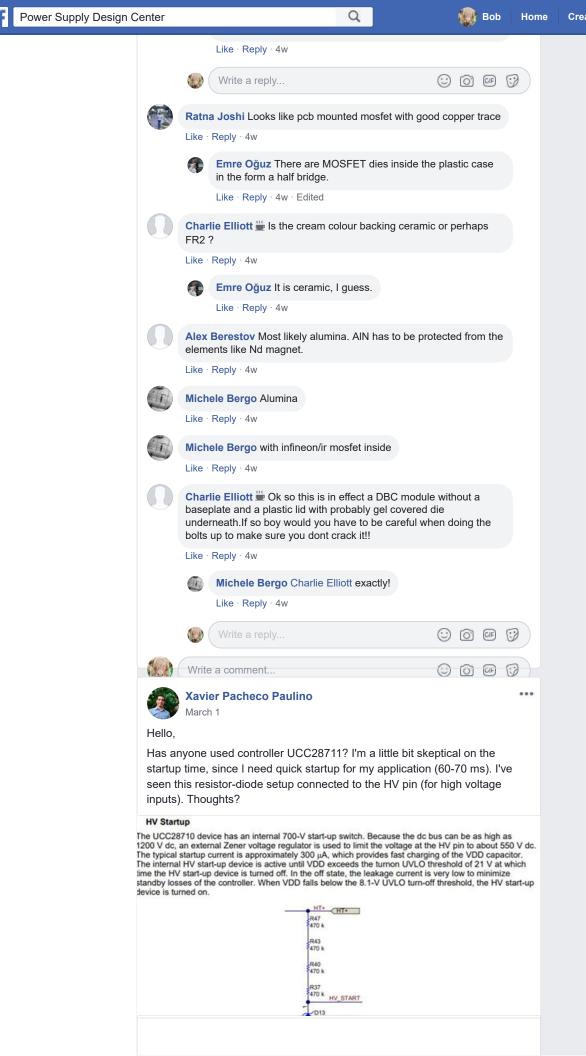


Emre Oğuz Yes, most likely the module comes from a SME driver. But I am not interested in motor driver itself. I am searching for a packaging company which produce small footprint MOSFET modules like this one.

Like · Reply · 4w



Michele Bergo they are producing the modules themselves



Home



Q







Bob White In what document did you find "Fig 16 HV Startup Circuit"?

Like · Reply · 4w



Xavier Pacheco Paulino In this app note: http://www.ti.com/lit/ug/tidu412b/tidu412b.pdf

Like · Reply · 4w



Bob White Wow, a quick look and I immediately found a very, very wrong statement - Figure 3 and the last paragraph of page 4. TI data sheets and app notes often have little mistakes but not usually this bad.

Like · Reply · 4w



Xavier Pacheco Paulino Bob White What's the wrong statement?

Like · Reply · 4w



Bob White Xavier Pacheco Paulino Do you really get 1800 V rating with 900 V MOSFETs arranged in cascode as shown? Tell me why not.

Like · Reply · 4w



Xavier Pacheco Paulino Well, we don't want to hit the max VDS. They didn't apply a derating factor.

Like · Reply · 4w



Bob White Xavier Pacheco Paulino Not even close. Try again.

Like · Reply · 4w



Bob White OK, I need to call it a night so here is the answer (sort of).

All voltage referenced to the primary common/return.

Suppose there was 1000 V on the drain of Q2 and that Q2 and Q1 split the voltage equally (a bad assumption but we will go with it for now).

What is the voltage on the drain of Q1?

What is the voltage on the source of Q2?

What is the voltage on the gate of Q2?

What is the gate to source voltage of Q2?

Is there a problem here?

Like · Reply · 4w



Write a reply...











Col Johns Bob White ZD2/D13 is 550V per fig 16 - this is how the cascode works ... Fig6 shows the G-S zener (15v) to protect the top fet ... sharing resistors a good idea though ...

urawn incorrectly... must throw a lot of people

Like · Reply · 4w



Nathan Ellis Darrell Hambley Agreed; You need the additional Vgs zener across M2 so its source doesn't drop ~500V below its gate when M1 turns on.

Turn-off will still be problematic though; the resistor adjoining both zener cathodes proximal to the gate of M2 (Fig.6) will want to be small to allow M2 to turn off quickly as its source shoots up and reaches 500V (Cgs charge needs to bleed off into left-of-center 500V zener reference). However, a small resistor here implies HUGE quiescent current draw when M1&M2 are on.

Could actually probably solve this by using a larger resistor here (for low quiescent draw when ON) and putting an additional diode in parallel with that resistor with its cathode pointing to the left (Allows Cgs2 to dump out its charge as Vg2 goes higher than 500V).

Cascoding is a neat trick, but I would be very careful here.

Like · Reply · 4w



Col Johns Nathan Ellis - the current is not huge, I think, as limited by the upper resistors (~2Meg) ... the gate R is typ 10 ohm...

Like · Reply · 4w · Edited



Nathan Ellis Col Johns Aha, I see; so the 500V zener doesn't hold a constant 500V across it because the Vgs-zener outweighs it when M1 is on 🍐 In that case it seems as if you wouldn't theoretically need the resistor at all? (Other than to add some damping)

Would think you'd want to do some capacitor feed-through analysis to ensure M2 turns on fast-enough with M1: If you assume zero parasitic capacitance (other than Cgs2), M2 turns on with an RC time constant of ~(2Mohm)\*(Cgs2) slooooowwww... And if it turns on at much slower rate than M1 then it will have the full 1000V across it for a short time. The (Cdg2+Czener)-Cgs2 capacitor divider might have it pop on nicely though.

Edit: That's also a lot of CV^2f loss across the 500V zener, but perhaps tolerable for high power throughput.

I still think this would be very finicky to dial in: seems all like a balancing act with low tolerance to component variation. Thoughts?

I bet there are more robust (albeit more expensive) alternatives

I'm also not sure if there's really any advantage to doing this; the device physicists already build devices with "pseudocascode" i.e. drain extending or NMOS+J-FET. Is this just motivated by a high-voltage device availability issue? (I haven't seen any derivations showing that a 50/50 voltage split cascode is more efficient than a 10/90 split).

Like · Reply · 4w · Edited



Col Johns This ckt has in fact been employed quite widely by power integrations devotees - often the 550V zener is split into two with a 33pF cap across each to provide a bit more oomph at turn on, depending on Cgs these caps might be recharged when the lower device turns off ... the volt split is not exact and for very low Vin the lower device does all the

Given that 2 x 600 or 2 x 800V fets are quite cheap compared to 1200 / 1600 volt device - the approach is attractive for low cost metering power supplies for 3 phase ... Nathan Ellis

Like · Reply · 4w · Edited



Nathan Ellis Col Johns Cheers Col, thanks for the insights.



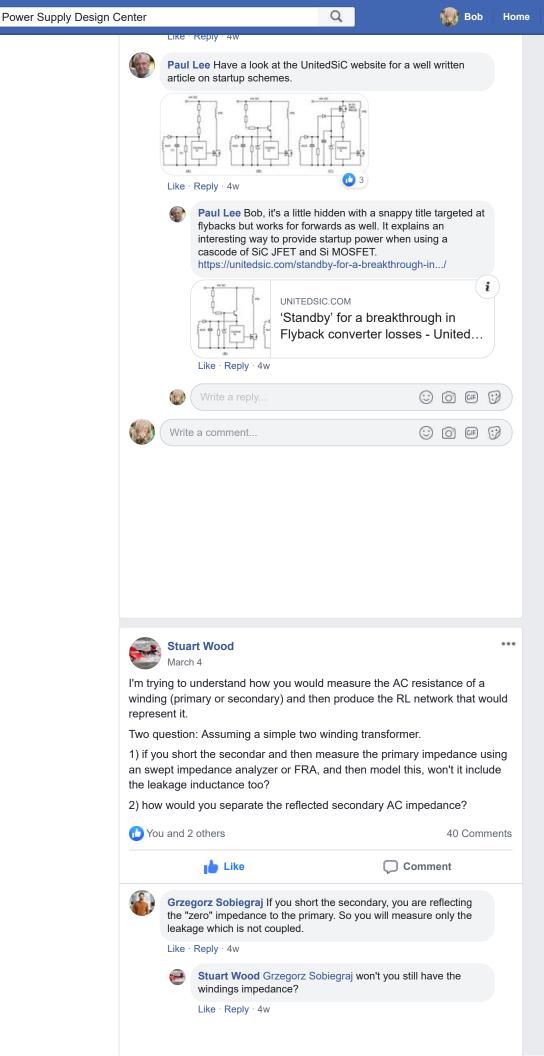


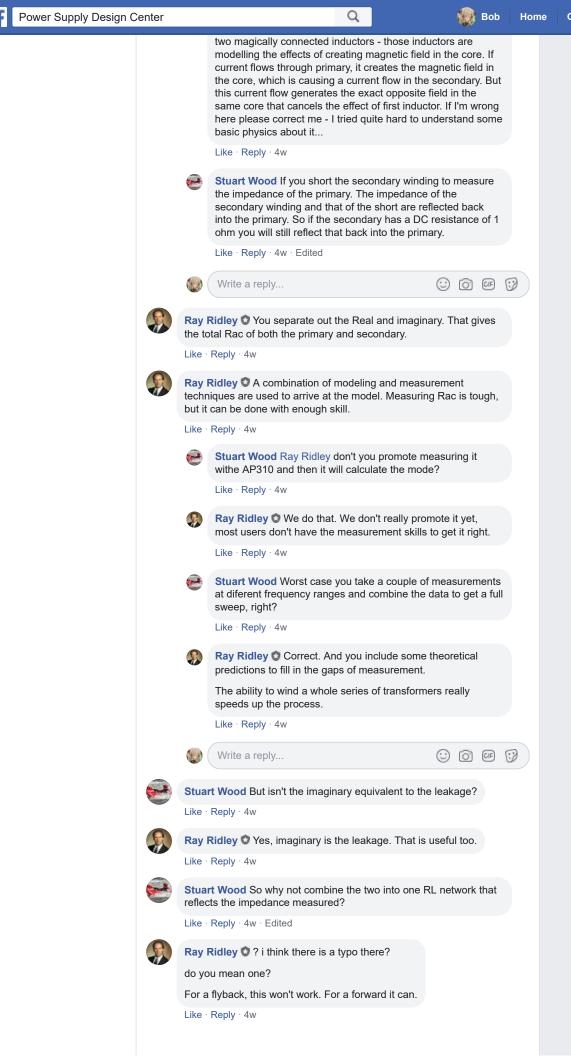














resistance into the one complex INL network instead of braking out the leakage inductance into its own circuit element

Like · Reply · 4w



Ray Ridley • We have all sorts of techniques for doing this. For example - build a transformer with two identical primaries instead of a secondary.

Then as a good approximation, you will measure 2x the ac resistance.

Then do the same with two secondaries. Not as easy if the turns count is low, which is why it is good to have analysis to back up the measurements, and vice versa.

Like · Reply · 4w



David Edwards You can see the ac resistance of just one winding by removing the core then measuring the winding.

Also, with the core intact and the other winding shorted AND if your impedance analyzer goes low enough in frequency, at low frequencies you should see the ac resistance of just the winding under measurement, then, as the test frequency increases, at some point you should see a step in ac resistance as magnetic coupling puts the two windings in series.

Like · Reply · 4w



Ray Ridley This is another technique that we often use. You have to be careful though, the windings will talk to each other and affect what the ac resistance actually is.

Like · Reply · 4w



Ray Ridley Vou almost have to use that technique for inductors.

Like · Reply · 4w



**Stuart Wood I** just was looking at paper for measuring the AC resitance of inductors using a second winding. I'll try and post it tomorrow.

Like · Reply · 4w



Stuart Wood Https://ieeexplore.ieee.org/document/8291492



IEEEXPLORE.IEEE.ORG

A New Method for Measuring Winding AC Resistance of...

Like · Reply · 4w



Ray Ridley Yep that is another technique we use. Put a hard short in the inductor in the right place, we use foil for this. The model is easy, so you can extract that part afterwards.

the Utah State University Power Electronics Laboratory, I am able to share what I have learned. The key to understanding this is learning how to measure and model mutual impedances. Power electronics engineers are typically familiar with mutual inductances, but few are familiar with mutual resistances. Consider what happens when you measure the series resistance and inductance of a transformer winding with all windings open. Both the inductance and resistance are high. If you short a winding and measure the inductance at another winding, both the inductance and the resistance are reduced considerably. From a circuit theory point of view, the reason is that there is both a mutual inductance and a mutual resistance which nearly cancel the open circuit inductances and resistances of the measured and shorted windings. From a magnetic point of view, the current in the shorted winding largely cancels the field produced by the measured winding and this reduces the losses. Dowell figured out how to quantify that effect and others have figured out how to create LR networks to represent it. However, this approach only works when there are one or more primary windings connected in series and one or more secondary windings connected in series, and the magnetizing current is small. The Dowell analysis depends on equal and opposite amp-turns, so it can't model the open-load ac resistance. Now suppose there are windings connected in parallel, or multiple secondary windings with independent loads. For those cases, the MMF diagram is indeterminate and another approach has to be used because the ac resistances depend on the current distributions, which can't be known in advance. About 20 years ago, I found that this issue had been thoroughly studied by a few authors in the utility industry, and I learned how to apply their techniques to the the magnetics used in power electronics. Here are two key papers: (1) Electrical terminal representation of conductor loss in transformers. (This discussed mutual impedances. The author was not in the utility industry.) https://ieeexplore-ieeeorg.dist.lib.usu.edu/document/60685 (2) New power transformer model for the calculation of electromagnetic resonant transient phenomena including frequency-dependent losses. (This model shows how model mutual impedances in a circuit simulator.) https://ieeexplore-ieee-org.dist.lib.usu.edu/document/847246 My work has been done in Mathcad, but I'm getting assistance translating it to Excel, and I hope to get it translated into Matlab scripts soon as well. I would be glad to correspond with anyone who wants to learn more about this topic.

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Like · Reply · 4w



Alex Berestov What's the point of posting URL requiring USU login?

Like · Reply · 4w



Ray Ridley Can you please repost without the login Bryce Hesterman?

Like · Reply · 4w



David Edwards . Hello Bryce Hesterman,

Everyone should read your groundbreaking work on the realizability of multiple coupling factors for a set of windings. It's importance was recognized by Mike Engelhardt and is used by LTspice to determine whether to issue error messages for unrealizably coupled windings.

Kudos aside, I can't help but believe that mutual resistance is naught but an unnecessary and misleading mathematical artifice. Models typically attempt to duplicate the behavior of a system with constant value lumped elements, but carrying this too far can be misleading.

For example, one would like to model transformer winding ESR as a constant. However, when other loss mechanisms (such as core loss) are inadvertently added into the ESR measurement (or model), it causes the overly simplistic ESR model to rise in value with frequency. The same can be true for eddy currents induced in other windings or nearby conductors.

Since mutual resistance does not really exist (as far as I know) it should not be used to explain transformer loss. Just my two cents.



And at the same time magnetics are absurdly simple. Anyone can learn to design and make them in just a few hours as we show in our workshops.

It's a wonderful paradox.

Like · Reply · 4w



Ray Ridley Not sure what you mean by ESR being constant. Obviously it rises with frequency.

Probably just a different way of looking at the same thing.

Like · Reply · 4w



## David Edwards @ Ray Ridley,

Many engineers tend to speak and write precisely, even pedantically, but it is surprising how difficult it is to avoid miscommunication.

My point is that engineers tend to like models built from invariant lumped elements. If measurement shows that the lumped element (for example, ESR) is not constant over all frequencies) then the model must be extended by appropriately adding more lumped elements.

This becomes problematic with systems that contain diffusionlike elements, such as skin effect, which really needs a half pole representation. Unfortunately, no half-pole lumped element exists, so one must resort to an approximation with RC or LR networks.

Like · Reply · 4w



Write a reply...











David Edwards Emember when Slobodan 'Cuk was touting the ripple reduction properties of his converter topology and he explained its workings using the mathematical artifice of negative inductance?

Of course, there is no such thing as a real negative inductance. It is a consequence of choosing a nonphysical, but mathematically valid solution to an under-determined problem with an infinite number of possible solutions. Dr. 'Cuk used each winding's inductance (without adjusting for turns ratio) and mutual inductance to come up with mathematically forced negative values for leakage inductance. With a solution that first adjusted for turns ratios, all inductances would remain positive.

I always thought Dr. 'Cuk's explanation was a "smoke and mirrors" attempt to impress the unwary with the supposed uniquely mystical ripple-cancellation properties of the 'Cuk converter. I was not impressed, but the controversy Dr. 'Cuk stirred up back then sure was a lot of fun. He was the Mohamed Ali of power electronics (for those of you who remember both 'Cuk and Ali).

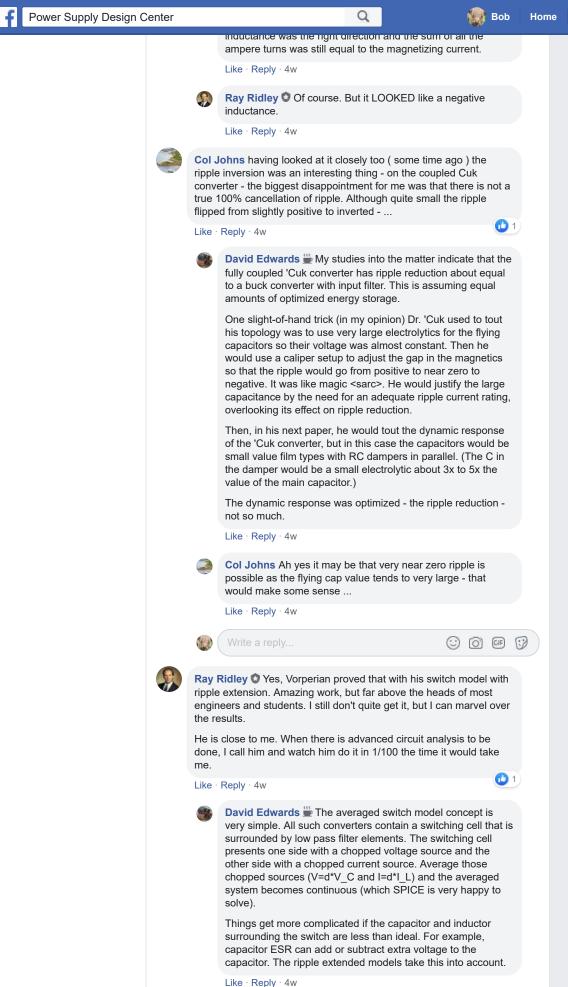
I suspect "mutual resistance", like negative inductance, is simply a mathematical artifice of a particular solution to an under-determined problem. It simply obscures rather than elucidates the underlying physical process. Other valid solutions with normal lumped elements that are much more closely tied to the underlying physical process should be possible. Note: this is just a gut-feel opinion - I could be completely wrong.

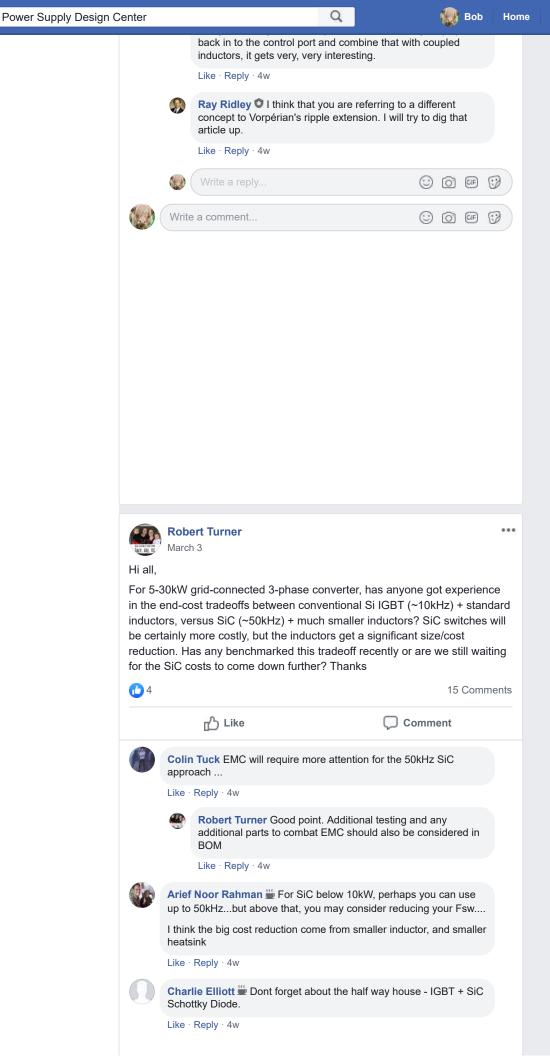
Like · Reply · 4w · Edited

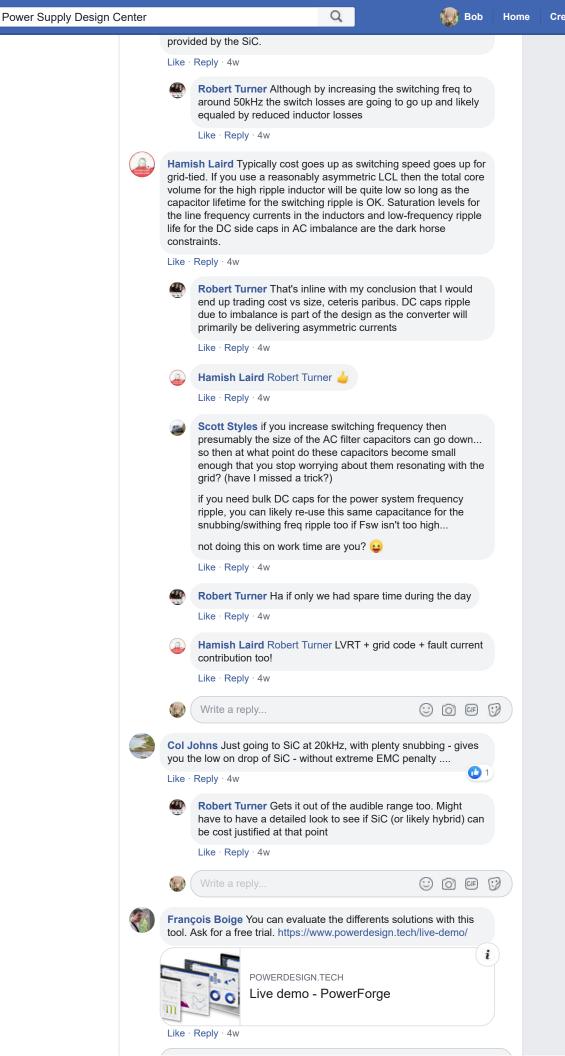


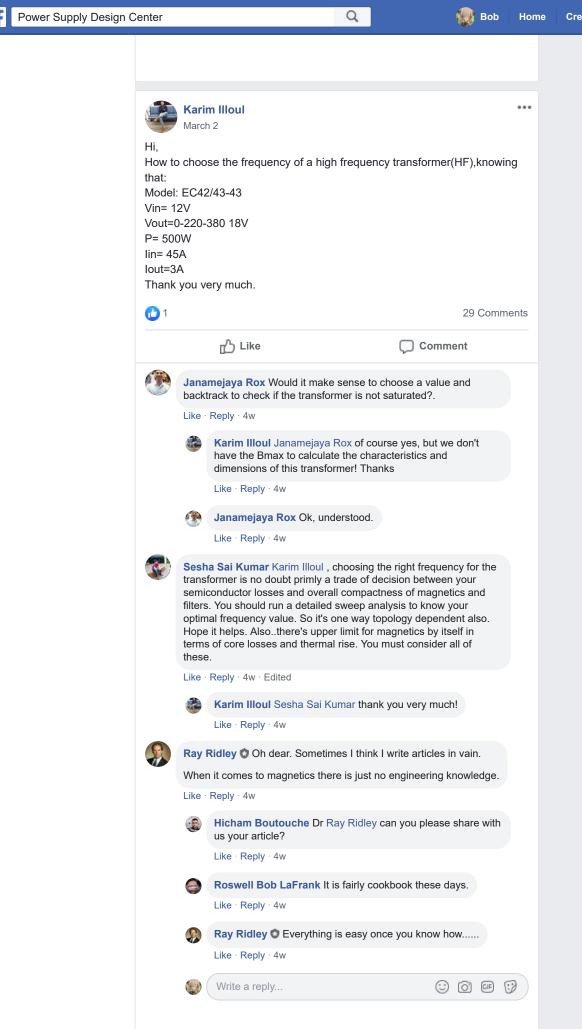
Ray Ridley VI remember looking at a converter in those days where the voltage on the winding was one polarity, and the current ripple was the wrong way. It was like cuks negative inductance. It can't exist on its own, has to be coupled to another winding of

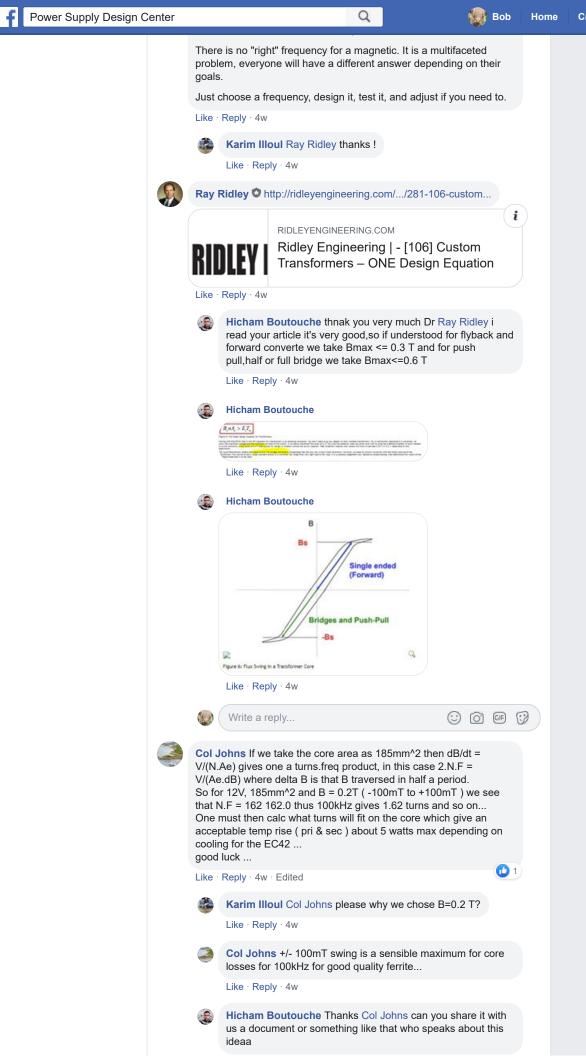
The waveforms were guite clear though - this was a negative inductance from a two-terminal point of view.

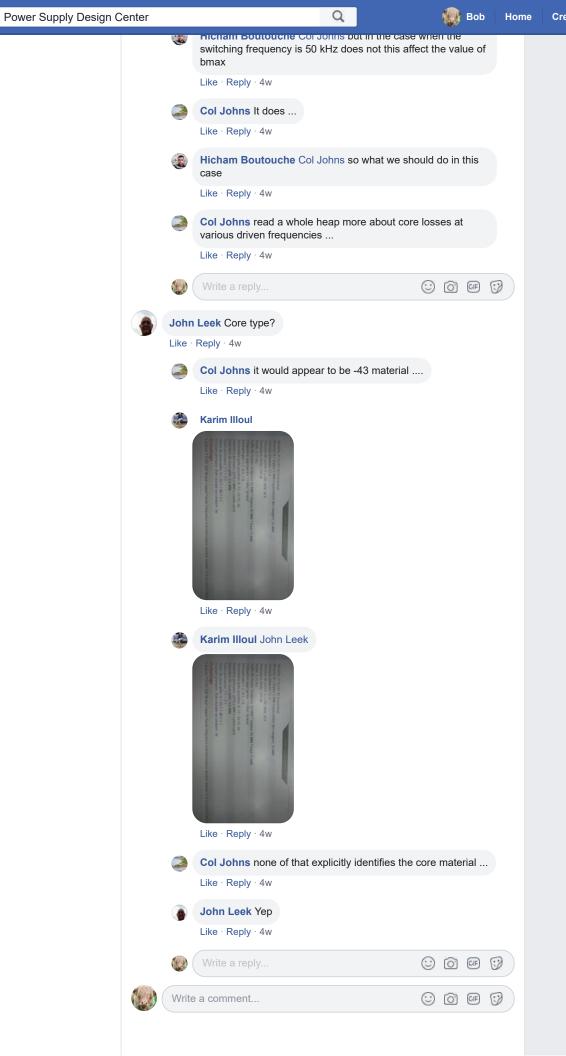




















Creep from gravity?

I am proposing using an existing board for a new project mounted vertically (due to the enclosure situation). There are large (25mm dia x 40mm ht) capacitors held onto the board with epoxy plus their own solder on 2 pins and some edge-mounted toroids 25mm tall. These older boards, normally mounted horizontally, have been through vibration with peaks in excess of 11 G's in all axis. The engineering manager has a "gut feeling" about long term creep due to gravity which may eventually pull the parts off the board. I've never heard of a creep issue but maybe someone has. Any thoughts?



10 Comments







Paul Shepherd 11G's is a great version of HALT testing. I assume the Engineering Manager isn't an ME? Testing to failure might get

Like · Reply · 4w



Peter Comrie Ordinary glass creeps but only a really tiny bit over decades so glass fibre may too but this would be over a much longer time frame than any life expectancy of any electronic equipment. Significant creep would only happen at very high stresses and temperatures where glass would start to flow - way beyond where electronic components (or solder) would behave normally.

Like · Reply · 4w



Charlie Elliott "You have to be careful with increased bleedout of heatsink compound if used at high temp and vertical.

Like · Reply · 4w



Colin Tuck If there are soldered and epoxied - there should be no issue - what is lifetime of product - 7 years? (life of electro) - they should be fine ...

Like · Reply · 4w



Colin Tuck metal creep is more of an issue in metal turbine blades -I have never heard of it in power electronics ...

Like · Reply · 4w



Darrell Hambley I'm looking for any odd documented case where, yes, large parts can start to move downward on a vertical board. Again, I've never heard of this. I have seen many consumer products with vertical boards (old TVs etc) that are still intact 25 years later. These have the same continuous 1G of vertical stress that my parts will have. My worry is that actual data and facts don't hold a candle to "gut feeling".

Like · Reply · 4w · Edited



Jonathan Beaver Ask him to define a test that would simulate that failure mode. Perhaps some number of hours at some multiple of regular gravity (centrifuge or just weights tied to it)? Coming at it from a different approach might help clarify the situation in their head.

Like · Reply · 4w



Colin Tuck Standard FRG-4 pcb can change shape if bent and heated - but the stresses required are usually above the norm ...



